CMS Pixel Chip PSI46 V2 Test Results

Cristian Gingu
Fermi National Accelerator Laboratory, Batavia, IL 60510
- July 2005 -

Introduction

This document is a technical report of the PSI46V2 chip wafer test results. Three wafers were tested, which are identified below as: wafer #3 (ID=XT4EF6T), wafer #4 (ID=XN4F4YT) and wafer #5 (ID=XM4F4ZT). The numbering starts from wafer #3 because there were other two PSI46V2 wafers tested and reported previously (February 2005).

Section 1 presents the testing procedure changes from the previous testing in February 2005. Section 2 reports the test results obtained. A comparison is made with PSI test results for two out of the three wafers.

1. Testing program review

The same hardware and software instruments as in previous test reports were used, but some new tests were added this time. The overall testing program flow is presented below. The new tests are in italics.

1. Interface board setup – I2C address, frequency, CAL, TRIG, TOKEN delays.
2. Power on PSI46V2 chip.
3. Measure misc. currents and voltages.
4. Download chip configuration – program all DAC register with default values and set all pixels enable bit and set all pixels trim bits 0x08.
5. Repeat step 3.
6. *Do token out test.*
7. *Do I2C test.*
8. *Do I-V curve test for Vana DAC register.*
9. Do DAC registers' linearity test.
10. Do Vcal and MaskTrim loop test for each of the 4160 pixels.
11. *Do data buffer test for each double column.*
12. *Do time stamp buffer test for each double column.*
13. *Do WBC test.*

All tests are executed in this order, regardless of the results of previous tests, with the following exceptions:

1. In step 5, if the digital or the analog current supply are <5mA or >105mA the chip testing is aborted.
2. In step 6 if token out test fails the chip testing is aborted.

The following is a short description of the new test introduced.

1.1. Token out test description

The implementation of this test follows PSI test procedure. Without any CAL and TRIG signals, a TOKENIN is sent and the analog readout is checked for the right number of analog ‘pulses’.

If the chip responds with the proper number of pulses (i.e. just ultra black, black and last dac) the message "TokenOut Test PASS" is print out in the report file. Otherwise one of the following error messages is print out:

1. "Algorithm error - test length <> 5" if there is a software type error.
2. "FIFO or scmd type error = 0x" if there is a hardware type error.
3. "Error - Wrong number of readout words: 0x" if the number of analog ‘pulses’ readout is not exactly 3.

1.2. I2C test description

The implementation of this test follows PSI test procedure, except that the outer loop for I2C addresses does not contains all 16 possible values, but only 0x00, 0x01, 0x02, 0x04, 0x08 and 0x0F. The inner loop for I2C addresses scans through all 16 possible values. The outer loop represents the I2C values driving the I2C pads of the chip. The inner loop represents the I2C address sent through the I2C interface of the chip when it is addressed. The register exercised in this test is the control register switched from ‘full speed’ to ‘half speed’. The test is checking for a proper number of analog ‘pulses’ both when I2C pad address is equal with I2C interface addressing and when it is not equal. The PASS/FAIL results are encoded in a six element array, one for each of the 0x00, 0x01, 0x02, 0x04, 0x08 and 0x0F I2C pad addresses tested (see Figure 1). The number written in any of these six locations is a long integer number of 19 bits. These 19 bits represent:

1. Bit x= 0 to 15 is ‘1’ if there is a response error while I2C interface address is x.
2. Bit 16 is reserved for software type errors.
3. Bit 17 is reserved for hardware type errors.
4. Bit 18 is set to ‘1’ when PSI response length is > 255.

A report example for this test looks like in Figure 1. Note that all chips on these three wafers passed this test.

I2C Test Report
I2C_Result(I2Cpadadd=0)=0 0000000000000000000
I2C_Result(I2Cpadadd=1)=0 0000000000000000000
I2C_Result(I2Cpadadd=2)=0 0000000000000000000
I2C_Result(I2Cpadadd=4)=0 0000000000000000000
I2C_Result(I2Cpadadd=8)=0 0000000000000000000
I2C_Result(I2Cpadadd=15)=0 0000000000000000000

Figure 1 I2C test report example

1.3. Description of I-V curve test for Vana DAC register

The implementation of this test follows PSI test procedure. In a first step, the analog power supply current is measured for the following Vana DAC settings: 0x20, 0x40, 0x60, 0x80, 0xA0, 0xC0. This step is used to find, with a 0x20=32 setting precision, the DAC values for which the current is less than and also greater than 24mA. Then, in a second pass, a half interval algorithm is used to find with one LSB precision the DAC settings for which the current is ~24mA. There is no PASS or FAIL report for this test. The measured currents are just reported as in Figure 2.

I-V Curve of Iana Test Report
Iana measured currents are:
1.29mA
3.41mA
8.75mA
18.53mA
34.28mA
54.09mA
25.89mA
21.31mA
23.2mA
24.26mA
23.72mA

Figure 2 I-V curve test report example

Of course, the last Vana DAC setting is used for all the tests that follow. We found out that after this test we need to redo step 4 from our test sequence (download chip

configuration). This is due probably to the fact that for low Vana DAC register setting the configuration information of each pixel cell is lost.

1.4. Data buffer test description

The implementation of this test follows PSI test procedure. This test is repeated for each double column. In a first step 32 good pixels are searched to be all either in the left column or in the right column of the double column. This can be done since at this test moment we already have the information about each of the 4160 pixels. The reason for my request to have all 32 pixels in the same column is two fold. The first reason is to avoid software complications related to PSI calibration mechanism which enable the calibration for pixels at intersections of all column and row addresses that are calibrated. The second reason is more qualitative, in the sense that if there are more than 48 bad pixels in a column (out of the total 80 pixels), that column is already a pore one and we might want not to use such a chip and thus this test becomes somehow irrelevant.

Like in previous tests, I'm counting the number of analog 'pulses' to decide if the double column PASS or FAIL this test. For example, if I do calibrate x pixels (x>=0 and x<=31) I should see a corresponding number of hits in the readout. If x=32, there must be no hits in the readout, since the data buffer will reset. The test results are encoded in two arrays (see Figure 3a and 3b).

The first array, DBT_MiscErr is used to encode overall errors encountered. For each double column, it consists of a 7 bit long integer number used to encode errors as follows:

1. Bit 0 is reserved for software type errors.
2. Bit 1 is set when there are no 32 good pixels in neither left nor right column.
3. Bit 2 is reserved for hardware type errors.
4. Bit 3 is set when PSI response length is > 255 when x<>32.
5. Bit 4 is set when PSI response length is > 255 when x=32.
6. Bit 5 is set when PSI response length is <= 255 but not the right one when x<>32.
7. Bit 6 is set when PSI response length is <= 255 but not the right one when x=32.

A report example for this test looks like in Figure 3a.

Data Buffer Test Report

DBT_MiscErr(0) = 2	0 1 0 0 0 0 0
DBT_MiscErr(1) = 32	0 0 0 0 0 1 0
DBT_MiscErr(2) = 32	0 0 0 0 0 1 0
DBT_MiscErr(3) = 32	0 0 0 0 0 1 0
DBT_MiscErr(4) = 32	0 0 0 0 0 1 0
DBT_MiscErr(5) = 32	0 0 0 0 0 1 0
DBT_MiscErr(6) = 32	0 0 0 0 0 1 0
DBT_MiscErr(7) = 32	0 0 0 0 0 1 0
DBT_MiscErr(8) = 0	0 0 0 0 0 0 0

```
DBT_MiscErr(9) = 0        0  0  0  0  0  0  0
DBT_MiscErr(10) = 0       0  0  0  0  0  0  0
DBT_MiscErr(11) = 0       0  0  0  0  0  0  0
DBT_MiscErr(12) = 0       0  0  0  0  0  0  0
DBT_MiscErr(13) = 0       0  0  0  0  0  0  0
DBT_MiscErr(14) = 0       0  0  0  0  0  0  0
DBT_MiscErr(15) = 0       0  0  0  0  0  0  0
DBT_MiscErr(16) = 0       0  0  0  0  0  0  0
DBT_MiscErr(17) = 0       0  0  0  0  0  0  0
DBT_MiscErr(18) = 0       0  0  0  0  0  0  0
DBT_MiscErr(19) = 0       0  0  0  0  0  0  0
DBT_MiscErr(20) = 0       0  0  0  0  0  0  0
DBT_MiscErr(21) = 0       0  0  0  0  0  0  0
DBT_MiscErr(22) = 0       0  0  0  0  0  0  0
DBT_MiscErr(23) = 0       0  0  0  0  0  0  0
DBT_MiscErr(24) = 0       0  0  0  0  0  0  0
DBT_MiscErr(25) = 0       0  0  0  0  0  0  0
```

Figure 3a Data buffer test report example

The second array, DBT_HitResult, contains detailed test results for each of the 26 double columns using a 32 bit long integer number to encode failures. For example, if bit number X is ‘0’ then the double column PASS the test when X pixels were calibrated. A value of ‘1’ means FAIL. A report example for this test looks like in Figure 3b.

```
DBT_HitResult(0) = 2143289344   00000000000000000000111111111
DBT_HitResult(1) = 2146435072   00000000000000000011111111111
DBT_HitResult(2) = 2013265920   00000000000000000000000001111
DBT_HitResult(3) = 1879048192   00000000000000000000000000111
DBT_HitResult(4) = 2113929216   00000000000000000000000111111
DBT_HitResult(5) = 2013265920   00000000000000000000000001111
DBT_HitResult(6) = 1073741824   00000000000000000000000000001
DBT_HitResult(7) = 0            00000000000000000000000000000
DBT_HitResult(8) = 0            00000000000000000000000000000
DBT_HitResult(9) = 0            00000000000000000000000000000
DBT_HitResult(10) = 0           00000000000000000000000000000
DBT_HitResult(11) = 0           00000000000000000000000000000
DBT_HitResult(12) = 0           00000000000000000000000000000
DBT_HitResult(13) = 0           00000000000000000000000000000
DBT_HitResult(14) = 0           00000000000000000000000000000
DBT_HitResult(15) = 0           00000000000000000000000000000
DBT_HitResult(16) = 0           00000000000000000000000000000
DBT_HitResult(17) = 0           00000000000000000000000000000
DBT_HitResult(18) = 0           00000000000000000000000000000
DBT_HitResult(19) = 0           00000000000000000000000000000
DBT_HitResult(20) = 0           00000000000000000000000000000
```

DBT_HitResult(21) = 0	00000000000000000000000000000000
DBT_HitResult(22) = 0	00000000000000000000000000000000
DBT_HitResult(23) = 0	00000000000000000000000000000000
DBT_HitResult(24) = 0	00000000000000000000000000000000
DBT_HitResult(25) = 0	00000000000000000000000000000000

Figure 3b Data buffer test report example

1.5. Time stamp buffer test description

The implementation of this test follows PSI suggestions but it is, in our opinion, more comprehensive than their test procedure. The test is repeated for each double column. In a first step the first good pixels is searched for a given double column. Then a burst of 15 CAL pulses followed by a TRIG is sent to the chip and then the chip is readout and the response data length is checked. This sequence is repeated by moving the TRIG pulse such as to point to the first CAL of the burst, then to the second and so on. We must see in the readout just one hit in all these cases. When TRIG is pointing to the 13th CAL, the time stamp buffer is reset and we must readout no hit at all. See also the following oscilloscope picture for TOKENIN, CONTROL and ANALOG_OUT signals in Figure 4. The distance between two CAL pulses in the burst is 7*CLK period.

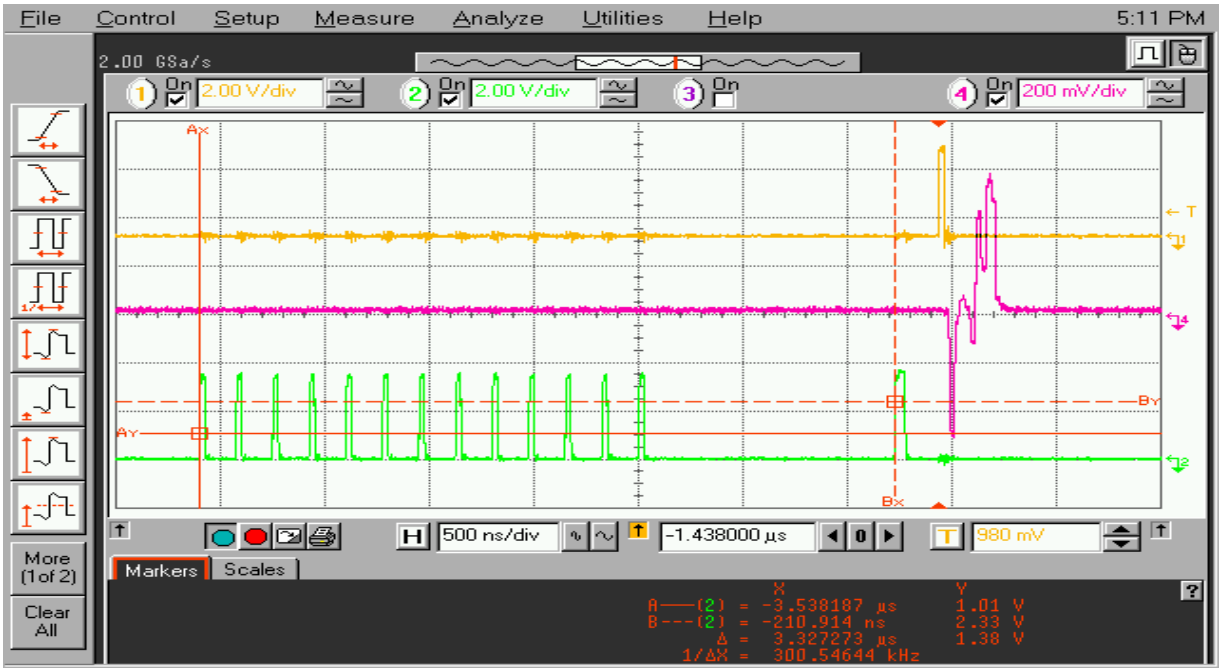

Figure 4 Time stamp buffer test waveform example

Like in the previous tests, I'm encoding the test results in a 26 location array of long integer TSBT_Result as follows:

1. Bit X= 0 to 11 is set to ‘1’ if there is a PSI response length error while TRIG pulse is pointing to the CAL pulse number X+1, otherwise the bit is ‘0’.
2. Bit 12 is set ‘1’ if there is a PSI response length error while TRIG pulse is pointing to the CAL pulse number 13 (buffer reset error).
3. Bit 13 is set ‘1’ when there is no good pixel found in the double column.
4. Bit 14 is reserved for hardware type errors.
5. Bit 15 is set to ‘1’ when PSI response length is > 255.

A report example for this test looks like in Figure 5.

Time Stamp Buffer Test Report

TSBT_Result(0)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(1)=4090	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(2)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(3)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(4)=2046	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0
TSBT_Result(5)=4746	0	1	0	1	0	0	0	1	0	1	0	0	1	0	0	0
TSBT_Result(6)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(7)=8132	0	0	1	0	0	0	1	1	1	1	1	1	0	0	0
TSBT_Result(8)=4062	0	1	1	1	1	0	1	1	1	1	1	0	0	0	0
TSBT_Result(9)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(10)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(11)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(12)=4094	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
TSBT_Result(13)=512	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
TSBT_Result(14)=1092	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0
TSBT_Result(15)=2792	0	0	0	1	0	1	1	1	0	1	0	1	0	0	0	0
TSBT_Result(16)=3514	0	1	0	1	1	1	0	1	1	0	1	1	0	0	0	0
TSBT_Result(17)=6416	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0
TSBT_Result(18)=3070	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0
TSBT_Result(19)=7208	0	0	0	1	0	1	0	0	0	0	1	1	1	0	0	0
TSBT_Result(20)=3948	0	0	1	1	0	1	1	0	1	1	1	1	0	0	0	0
TSBT_Result(21)=0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TSBT_Result(22)=6144	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
TSBT_Result(23)=5120	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
TSBT_Result(24)=506	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0
TSBT_Result(25)=4092	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Figure 5 Time stamp buffer test report example

It is worth to be outlined that, because of the calibration pulse circuitry inside the chip, this test is not working properly at clock frequencies higher than 5MHz. This was found after phone discussions with PSI group from Switzerland. All tests are performed at 40MHz clock frequency, the only exception being this time stamp buffer test.

1.6. WBC register test description

The implementation of this test follows PSI test procedure. This test is NOT repeated for each double column since the WBC register is only one general register in the chip architecture. In a first step the first good pixels is searched anywhere inside the pixel array, starting with the first chip column and row. On that good pixel the test is repeated for the following 8 values of WBC: 0x08, 0x09, 0x0A, 0x0C 0x10, 0x20, 0x40, 0x80. For each of these WBC settings, the CAL pulse position is fixed and the TRIG position is loop through all values between 0x08 and 0xF8. When the distance between CAL and TRIG matches the WBC number, a hit must be readout. No hit should be present in all the other cases.

Like in the previous tests, I'm encoding the test results in an eight location array of long integers WBC_Result as follows:

1. Bit 0 is reserved for software type errors.
2. Bit 1 is reserved for hardware type errors
3. Bit 2 is set when PSI response length is > 255.
4. Bit 3 is set when PSI response length is <= 255 but <>1 hit when TRIG == WBC.
5. Bit 4 is set when PSI response length is <= 255 but <>0 hit when TRIG <> WBC.

A report example for this test looks like in Figure 6.

WBC Test Report
WBC_Result(0) = 16 0 0 0 0 1
WBC_Result(1) = 16 0 0 0 0 1
WBC_Result(2) = 16 0 0 0 0 1
WBC_Result(3) = 0 0 0 0 0 0
WBC_Result(4) = 0 0 0 0 0 0
WBC_Result(5) = 16 0 0 0 0 1
WBC_Result(6) = 16 0 0 0 0 1
WBC_Result(7) = 16 0 0 0 0 1

Figure 6 WBC register test report example

1.7. Pixel scan test description

This is test 10 from the test sequence presented in Section 1. It is not changed from my previous implementations and it is shortly described here just for the record and for a better understanding of the results presented in Section 2. For more details please refer to previous reports from February 2005 and November 2004. Each of the 4160 pixels' responses is measured in a double loop scan of Vcal and MaskTrim registers as follows:

```
Pixel Test Report
Pixel Test Setup Parameters
masktrimmin =0x84
masktrimmax =0x90
masktrimstep=0x04
vcalmin     =0x40
vcalmax     =0xc0
vcalstep    =0x10
-------------------------------------------------------------
                LEV(min)        LEV(max)        RANGE           GAP
-------------------------------------------------------------
L1              1871            2000            129
L2              2047            2176            129             47
L3              2223            2336            113             47
L4              2399            2512            113             63
L5              2559            2688            129             47
L6              2719            2832            113             31
Q               2415            2672            257
-------------------------------------------------------------
PARAM           AVERAGE         MIN             MAX             ENTRIES
-------------------------------------------------------------
TVS             2.92            0               6               3367
TVI             164.61          133.33          208             3367
TVR2            0.91            0               1               3367
PED             2085            2082            2087            3367
UBK             1415            1413            1419            3367
BK              2013            2010            2015            3367
Q               2555            2444            2642            3367
CLev1           1926            1890            1966            1240
RLev1           1940            1888            1991            1537
CLev2           2097            2063            2139            1418
RLev2           2111            2059            2162            1854
CLev3           2267            2236            2293            1444
RLev3           2281            2232            2334            2086
CLev4           2437            2406            2462            1361
RLev4           2449            2403            2504            1970
CLev5           2603            2573            2630            756
RLev5           2615            2570            2669            1574
CLev6           2760            2732            2788            515
RLev6           2773            2730            2826            1080
-------------------------------------------------------------
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
-------------------------------------------------------------
COL1 found 29 defective pixels:ROW35N3,ROW39N3,ROW42N3,ROW46N3,ROW
COL2 found 31 defective pixels:ROW35N3,ROW39N3,ROW40N3,ROW46N3,ROW
COL3 found 21 defective pixels:ROW40N3,ROW42N3,ROW48N3,ROW53N3,ROW
```

Figure 7a Pixel test report example

1. Set the pixel mask bit ‘1’ (pixel enabled) and pixel trim bits to a default value masktrimmin. Set the Vcal DAC register to a default value vcalmin. Set this pixel to calibrate.
2. Start to increase Vcal in steps of vcalstep. Do chip readout at each step and check the result. If pixel responds with a hit, continue to step 3. If not loop on step 2 until the Vcal reaches the default vcalmax value and then continue to step 3.
3. Set Vcal to vcalmax and disable the pixel. Do chip readout and check the result.
4. Re-enable the pixel, set the Vcal to vcalmin, increment the trim bits with masktrimstep and jump back to step 2.

5. When trim bits reach masktrimmax this pixel exercise is complete. Execute clear calibration command and repeat the full test for a new pixel cell. Do this for all 4160 pixels.

This test is somehow different from the approach used at PSI. They do a similar but not identical trim sweep. Also, the other register involved in their test is not Vcal but Vthcomp.

A report example for this test looks like in Figure 7a and 7b.

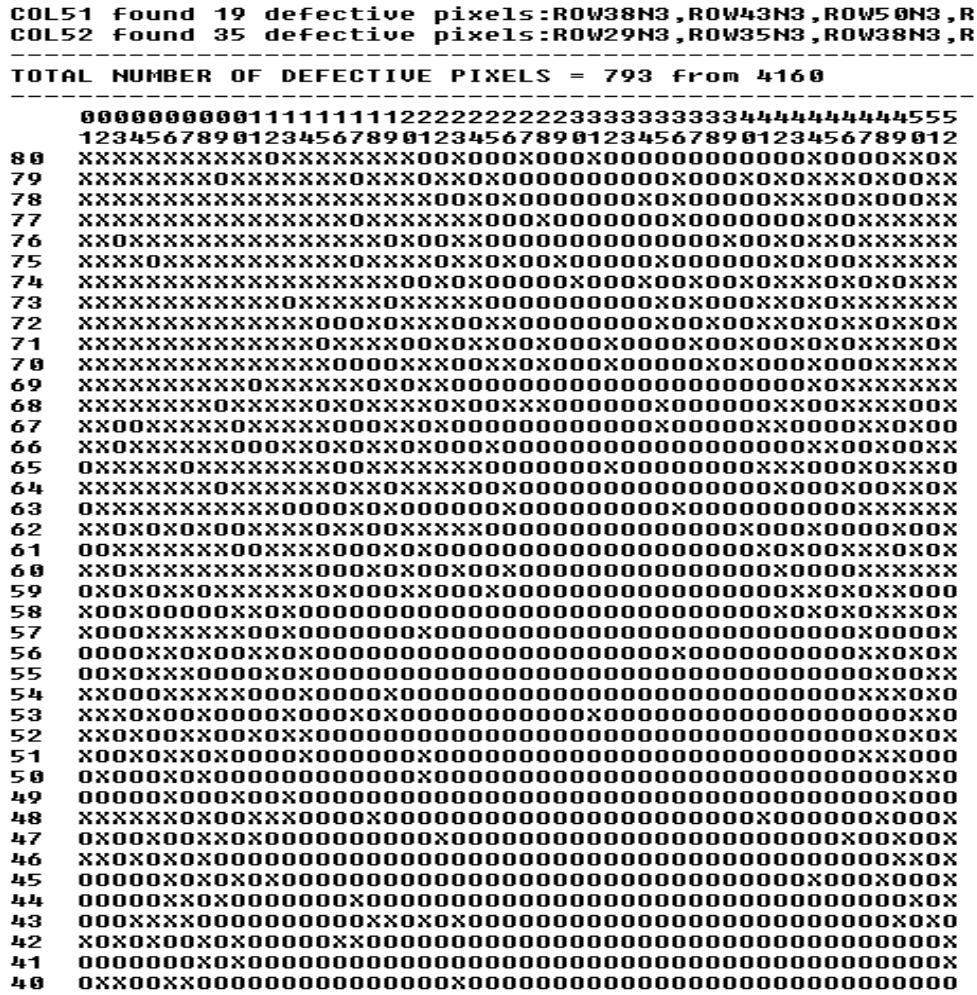

Figure 7b Pixel test report example

The L1, L2, L3, L4, L5 and L6 in Figure 7a represent the six analog levels used to encode the pixel's row and column address. The charge readout is Q. Both are represented in counts, after ADC conversion by the tester board. All measured pixels are included in this statistic. Then, after the pixel is qualified as good or defect (see previous testing reports for failure encoding) the lower part of Figure 7a shows the same six analog levels only on good pixels and separate for row and column addresses. Also the charge (Q), black, ultra black and

pedestal levels (BK, UBK, PED) are reported as well as the interpolation line's slope, intercept and correlation (TVS, TVI, TVR2) for the Vcal vs. trim bits dependence.

All the defective pixels are then listed, starting with first column and following a defect type encoding explained in previous reports. Then, as shown in Figure 7b, the total number of failed pixel is reported together with a pixel map of the chip. An 'X' symbol represents a failed pixel while a '0' symbol represents a pass pixel.

2. Testing results

2.1 Test report file description

The test report is a text file containing all test results as explained in Section 1. Currently there is one file for each chip. The first part of the file contains general information like date and time of testing, wafer ID, chip number and initial DAC register settings, as shown in Figure 8a. The chip numbering scheme is different from PSI scheme. The four chips inside a reticule are referred as _0, _1, _2 and _3 although within the pixel group community they are often called A, B, C and D respectively.

```
7/28/2005     12:46:58 AM Wafer#XM4F4ZT     Chip#44_1
Initial Settings (hex values)
adrsl      = 6
ncal       = 1e
ntrig      = a3
freq       = 11
tokendel   = 8
psdig      = 4400
psana      = 2b00
vdig       = 08
vana       = 90
vsh        = 80
vcomp      = 08
```

Figure 8a Test report example

At the end of the text file a brief summary of the chip failures is reported as in Figure 8b. The "FailCode" is a 14 bit long integer encoded as follows:

1. Bit 0 is set when digital current supply is too low.
2. Bit 1 is set when digital current supply is too high.
3. Bit 2 is set when analog current supply is too low.
4. Bit 3 is set when digital current supply is too high.
5. Bit 4 is set when DAC Linearity Test standard deviation is too low.
6. Bit 5 is set when DAC Linearity Test standard deviation is too high.
7. Bit 6 is set when DAC Linearity Test found a response length error.
8. Bit 7 is set when DAC Linearity Test found a FIFO full type error.
9. Bit 8 is set when Token Out Test failed.

10. Bit 9 is set when I2C Test failed.
11. Bit 10 is set when I-V Curve failed (currently not used).
12. Bit 11 is set when Time Stamp Buffer Test failed.
13. Bit 12 is set when Data Buffer Test failed.
14. Bit 13 is set when WBC Register Test failed.

```
************************************************************
FailCode=48  0  0  0  0  1  1  0  0  0  0  0  0  0  0
************************************************************
Failed Pixels per Double Column (1 to 26)
60 49 66 65 50 48 52 29 30 33 32 22 14 6 2 5 2 10 5 6 19 23 15 45 51 54
************************************************************
```

Figure 8b Test report example

There is also a new file I introduced. This is a file intended to give an overall view of all chips in a wafer or in different wafers, as can be seen in Figure 9. The minimum information that I found useful to have in this file is: date, time, wafer ID, number of total pixels failed, fail code as decimal number and as binary number.

```
7/27/2005 2:31:05 PM XM4F4ZT_1_0 1     FailCode=48    0 0 0 0 1 1 0 0 0 0 0 0 0 0 0
7/27/2005 2:35:09 PM XM4F4ZT_1_1 0     FailCode=48    0 0 0 0 1 1 0 0 0 0 0 0 0 0 0
7/27/2005 2:39:07 PM XM4F4ZT_1_1 191   FailCode=61920 0 0 0 1 1 0 0 0 0 0 0 1 1 0
7/27/2005 2:43:14 PM XM4F4ZT_1_3 0     FailCode=48    0 0 0 0 1 1 0 0 0 0 0 0 0 0 0
7/27/2005 2:46:40 PM XM4F4ZT_2_0 0     FailCode=48    0 0 0 0 1 1 0 0 0 0 0 0 0 0 0
7/27/2005 2:50:12 PM XM4F4ZT_2_1 3998  FailCode=61920 0 0 0 1 1 0 0 0 0 0 1 1 0
```

Figure 9 New Test report example

2.2 Row and Column analog level

The new test report described previously might contain some other parameter of interest. Then easy plots can be done by importing the text file in Excel and using the data sort utility.

For example, Figure 10a, b, c show the pixel's address levels for wafer #3, #4 and #5 respectively. Only chips with all pixels pass and FailCode=48 are presented. This fail code number 48 (bit 4 and 5 set) is present on all chips since, as it was mentioned in previous reports, some DAC registers have higher deviation from a best fit line. These are always Vbias_ph(0x13, pulse height differential ampl.) and Vbiar_roc(0x15, chip readout amplifier). From these three figures, the same conclusion outlined in previous reports can be inferred: it is NOT possible to use the same limits (min and max) for all six analog levels of all chips on a wafer. It might be possible to adjust the analog levels such as all (or at least most) of the chips will have analog levels within the same limits by having different settings for Vbias_ph and or Vbias_roc. This approach was not verified.

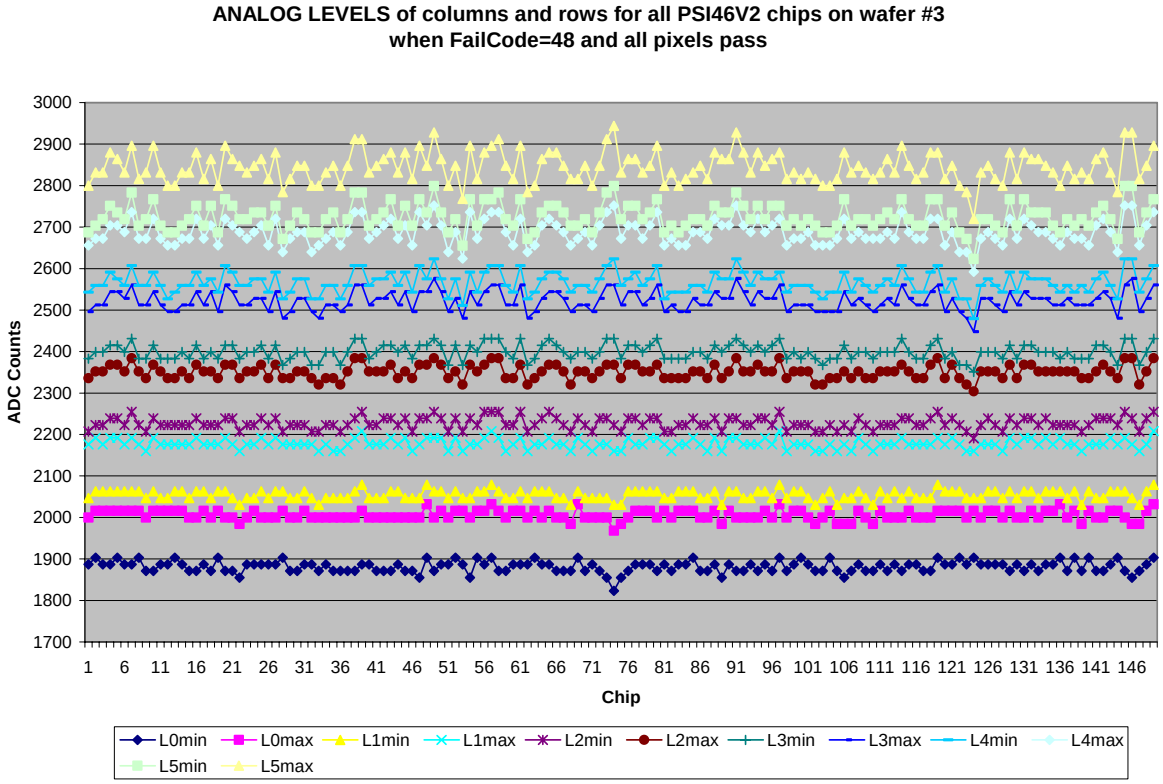

Figure 10a Analog Levels of pixel address on wafer#3

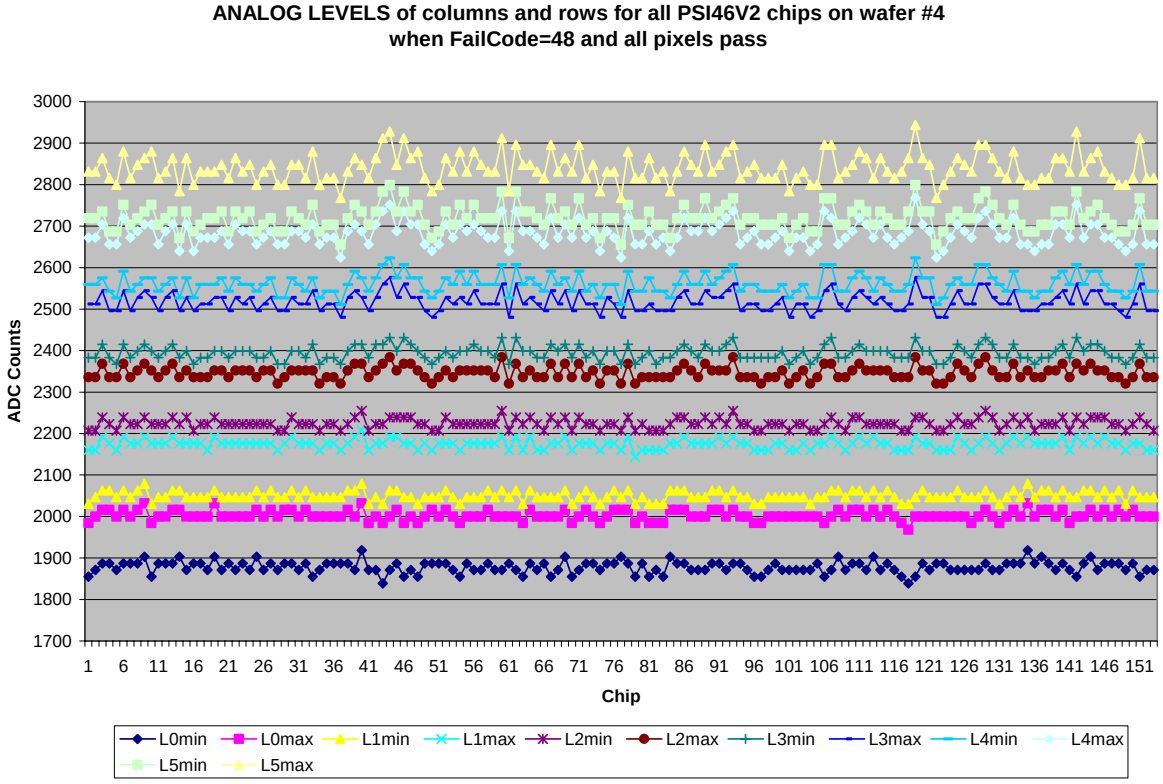

Figure 10b Analog Levels of pixel address on wafer#4

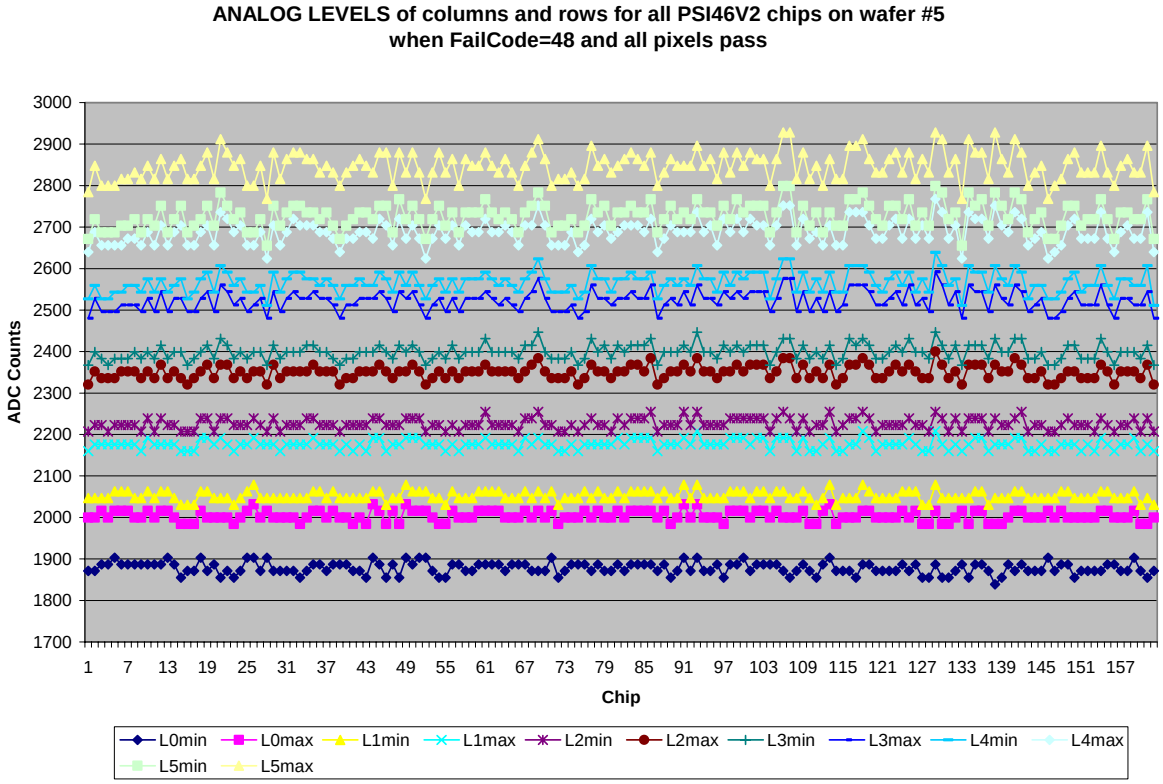

Figure 10c Analog Levels of pixel address on wafer#5

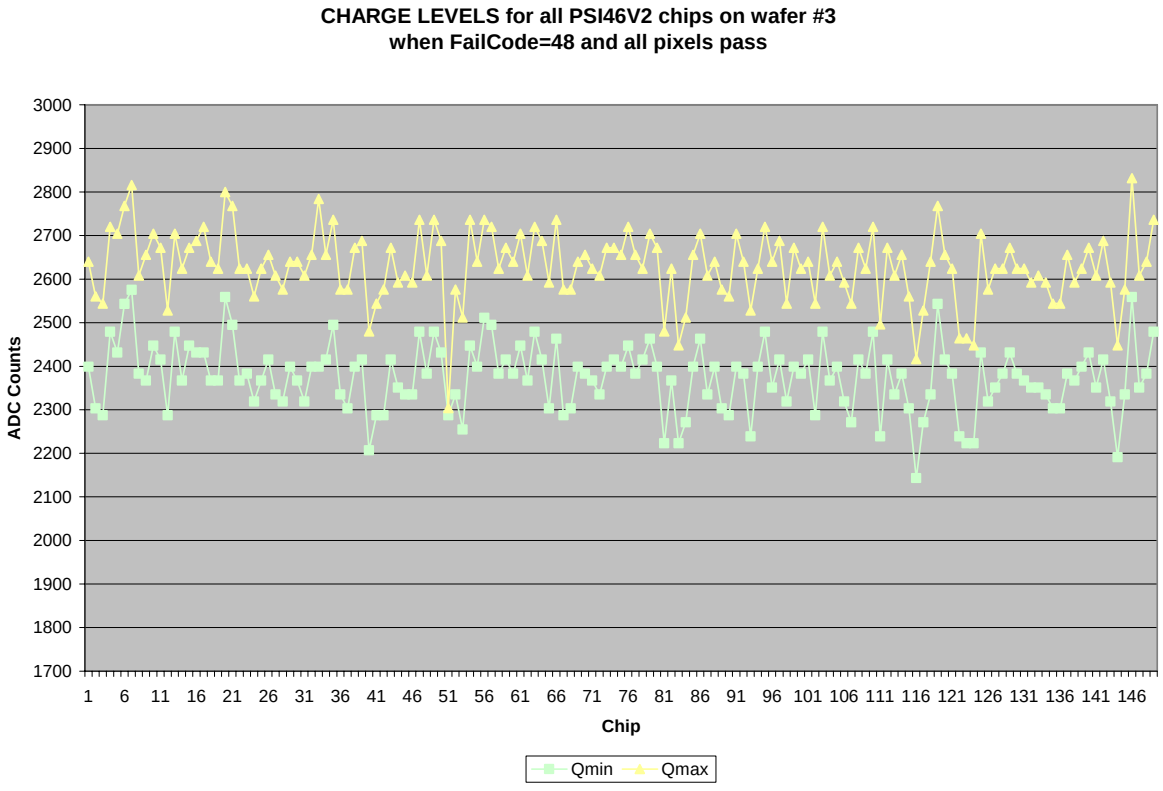

Figure 11a Pixel charge variation on wafer#3

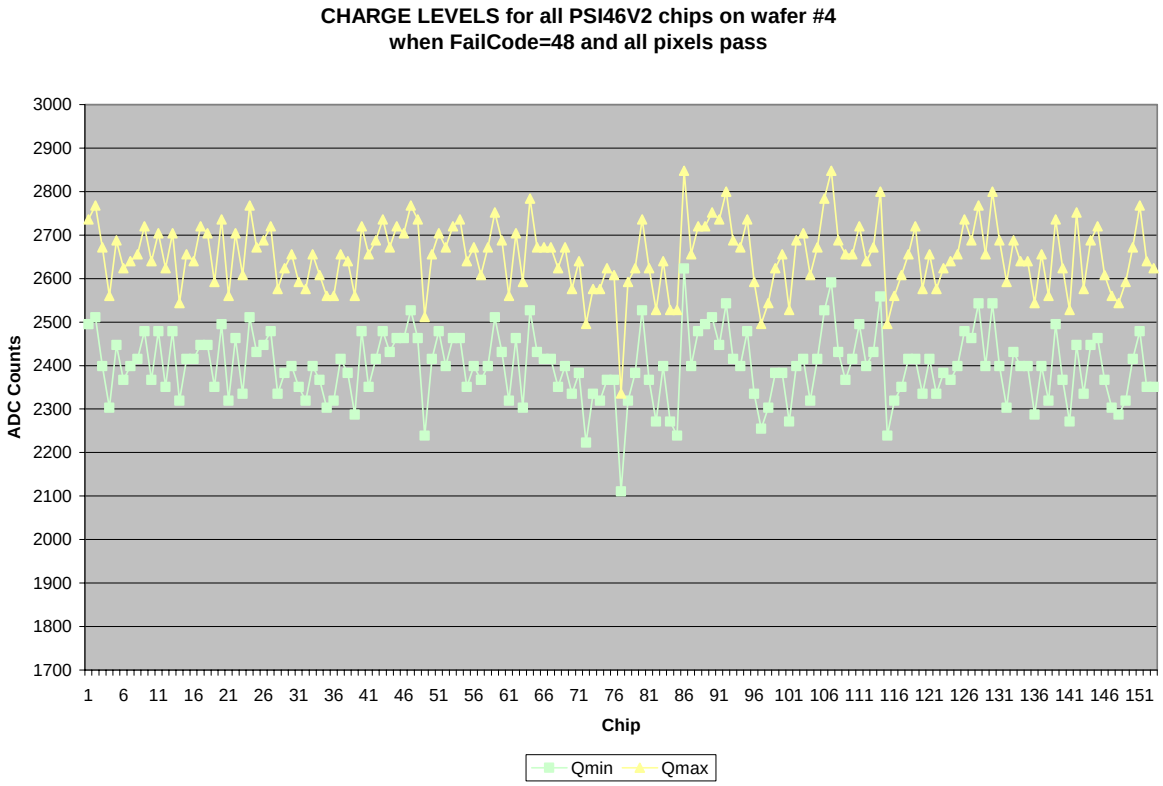

Figure 11b Pixel charge variation on wafer#4

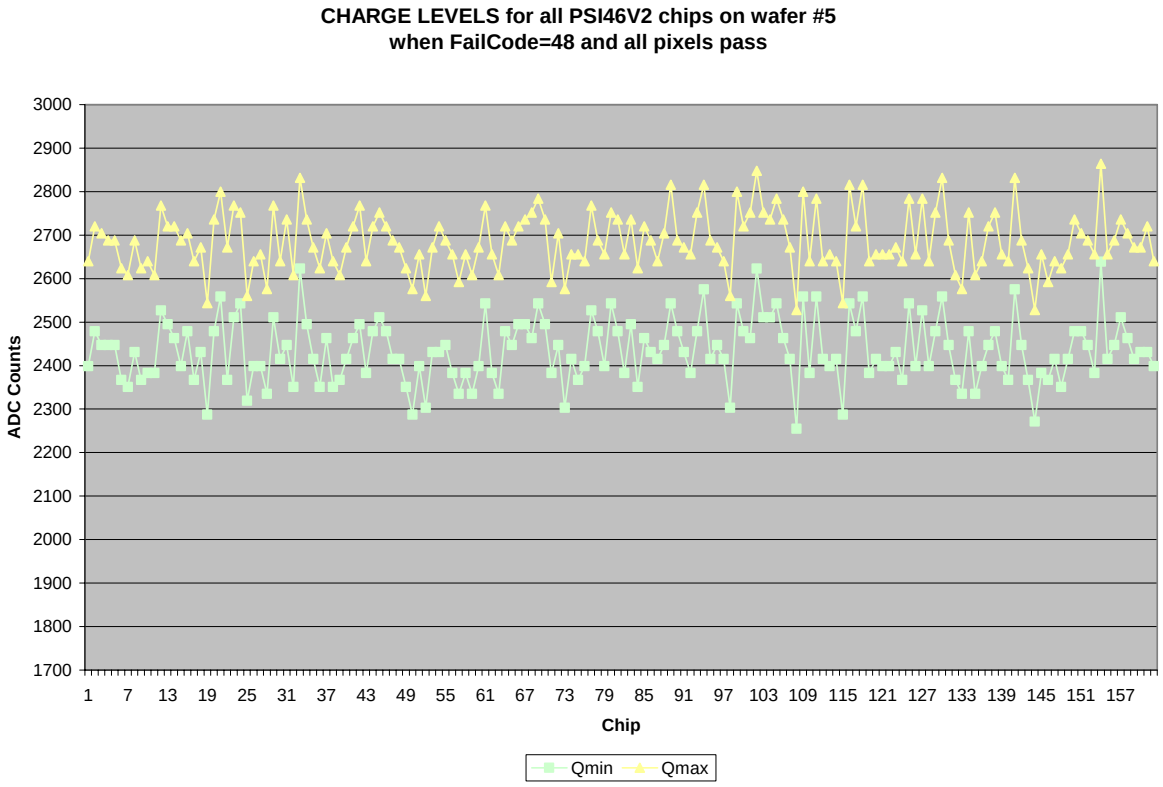

Figure 11c Pixel charge variation on wafer#5

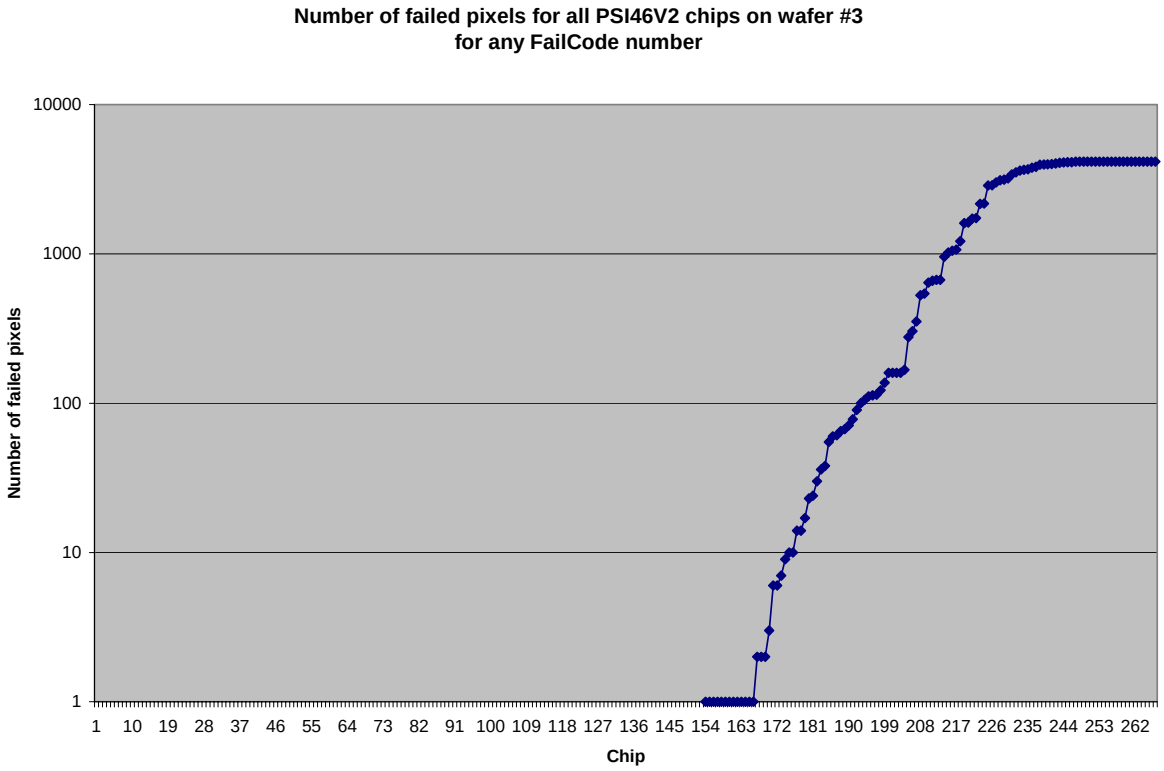

Figure 12a Number of failed pixels on wafer#3

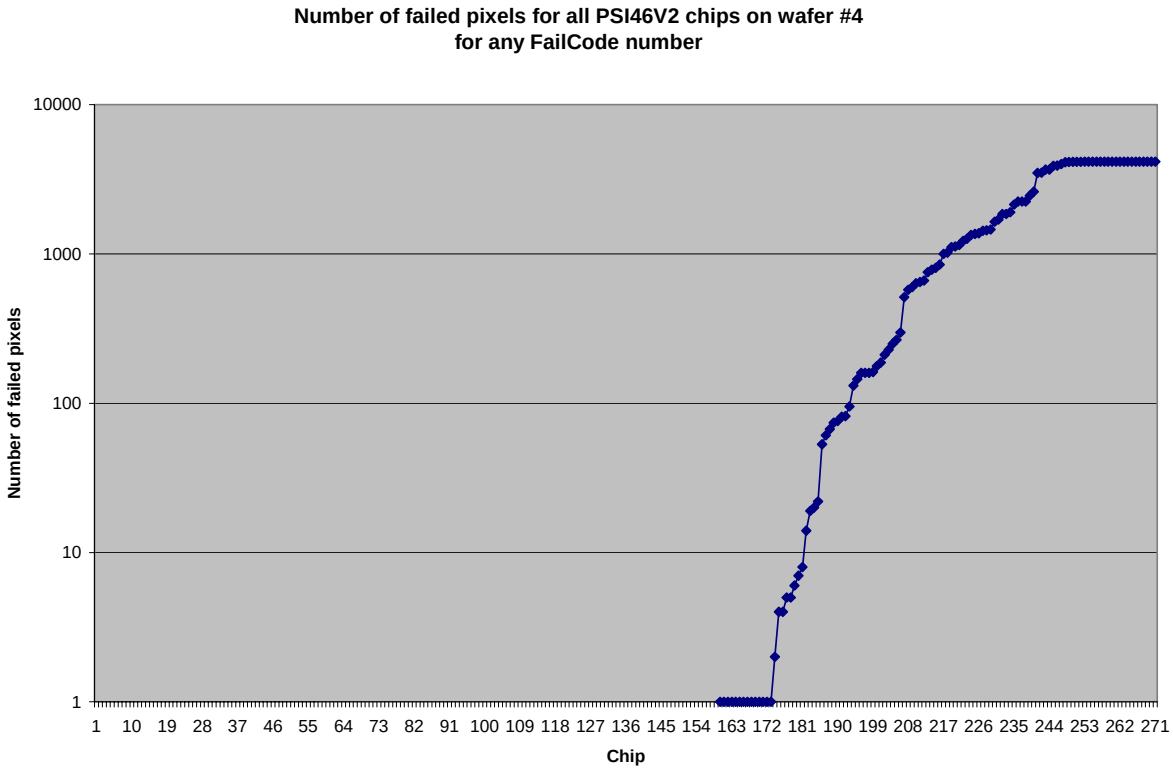

Figure 12b Number of failed pixels on wafer#4

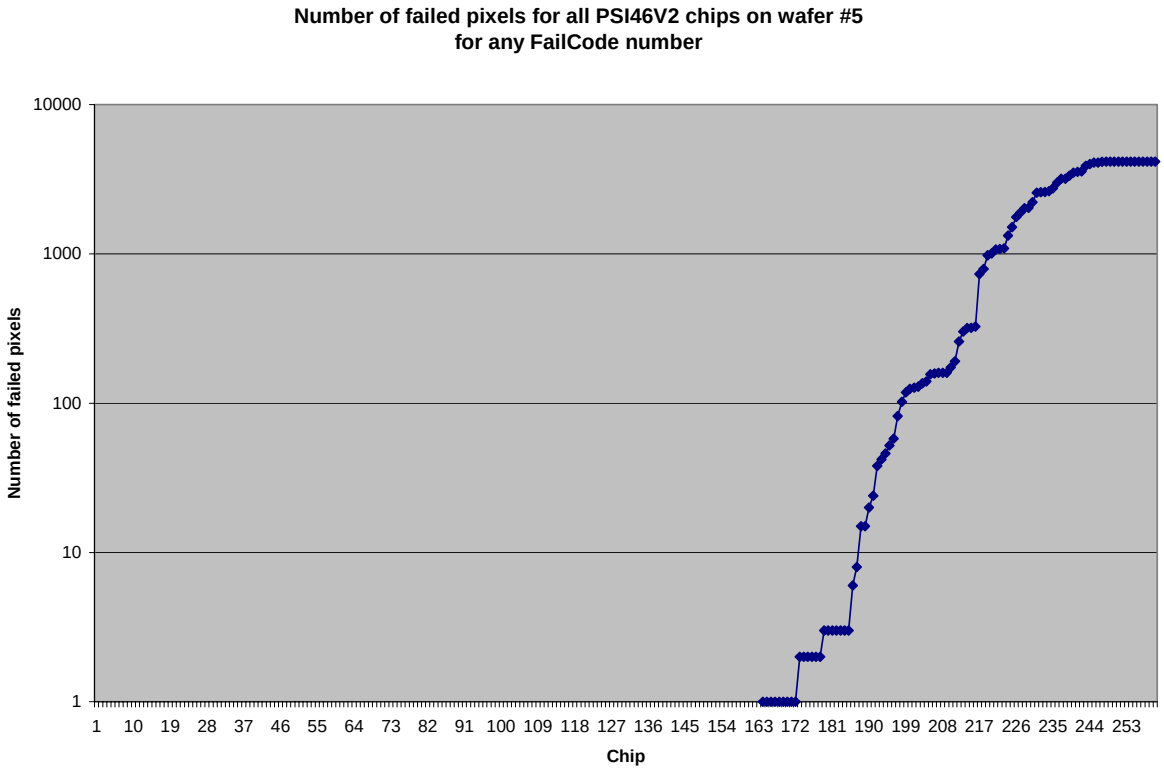

Figure 12c Number of failed pixels on wafer#5

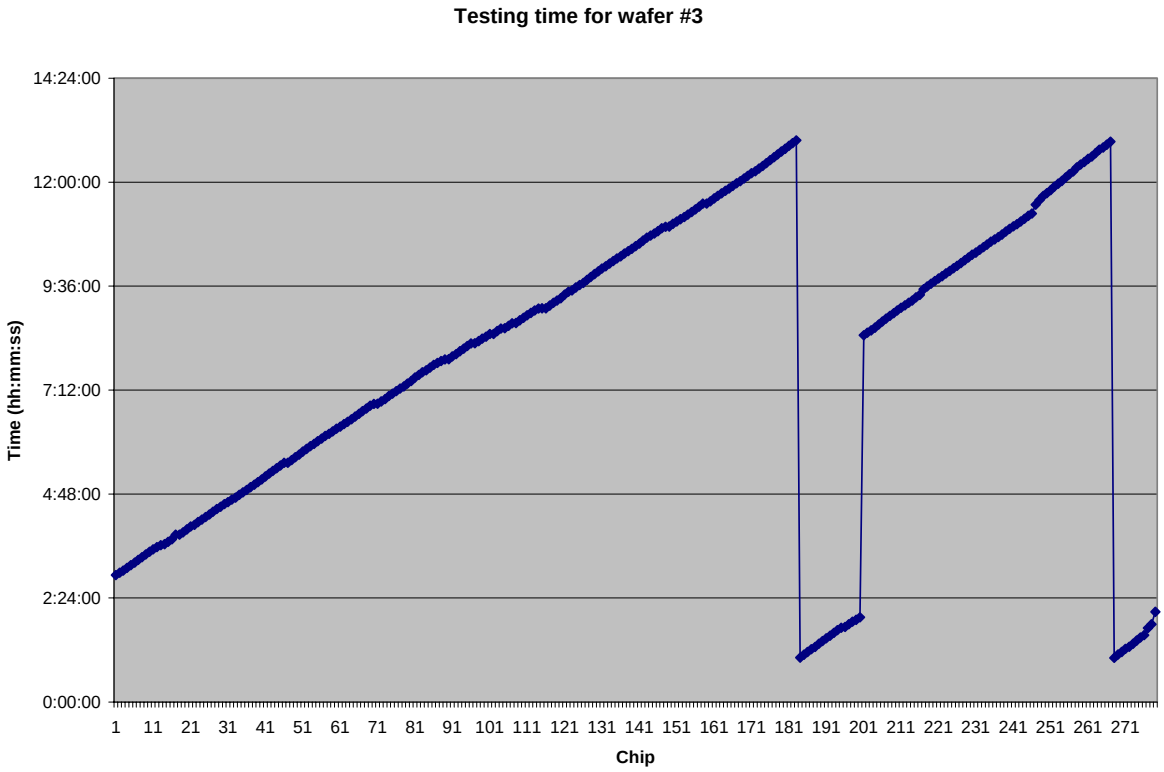

Figure 13a Testing time on wafer#3

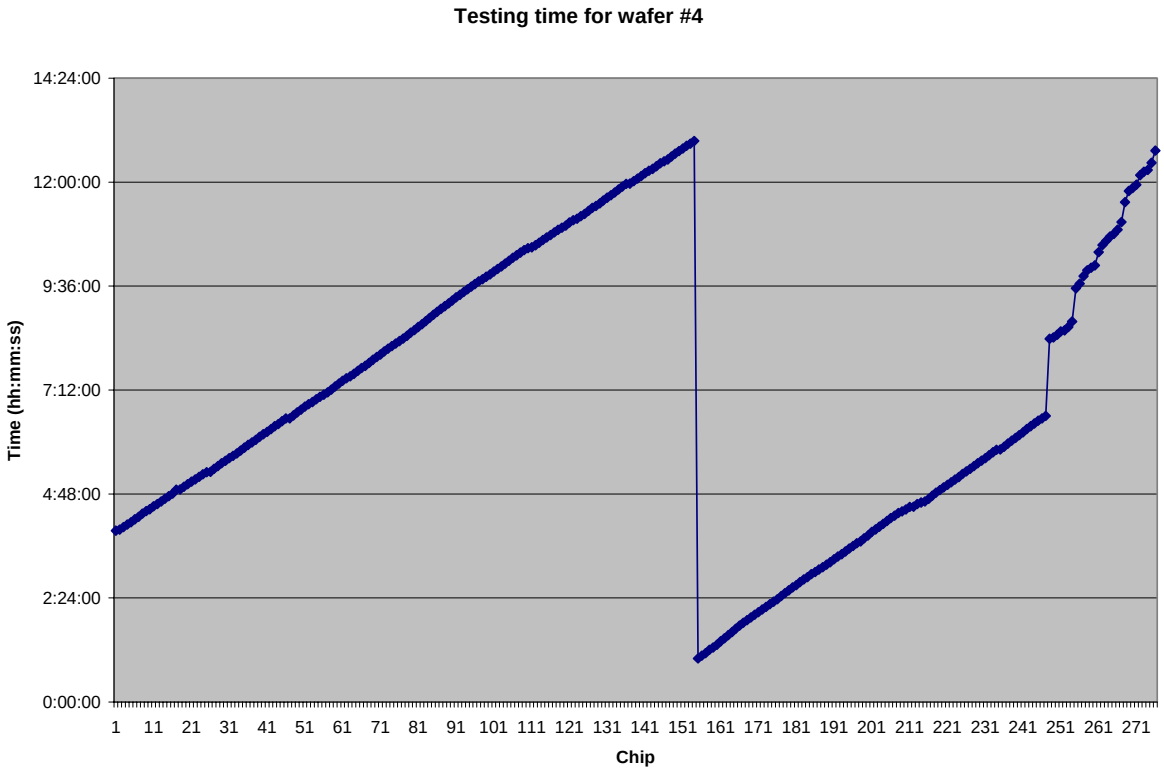

Figure 13b Testing time on wafer#4

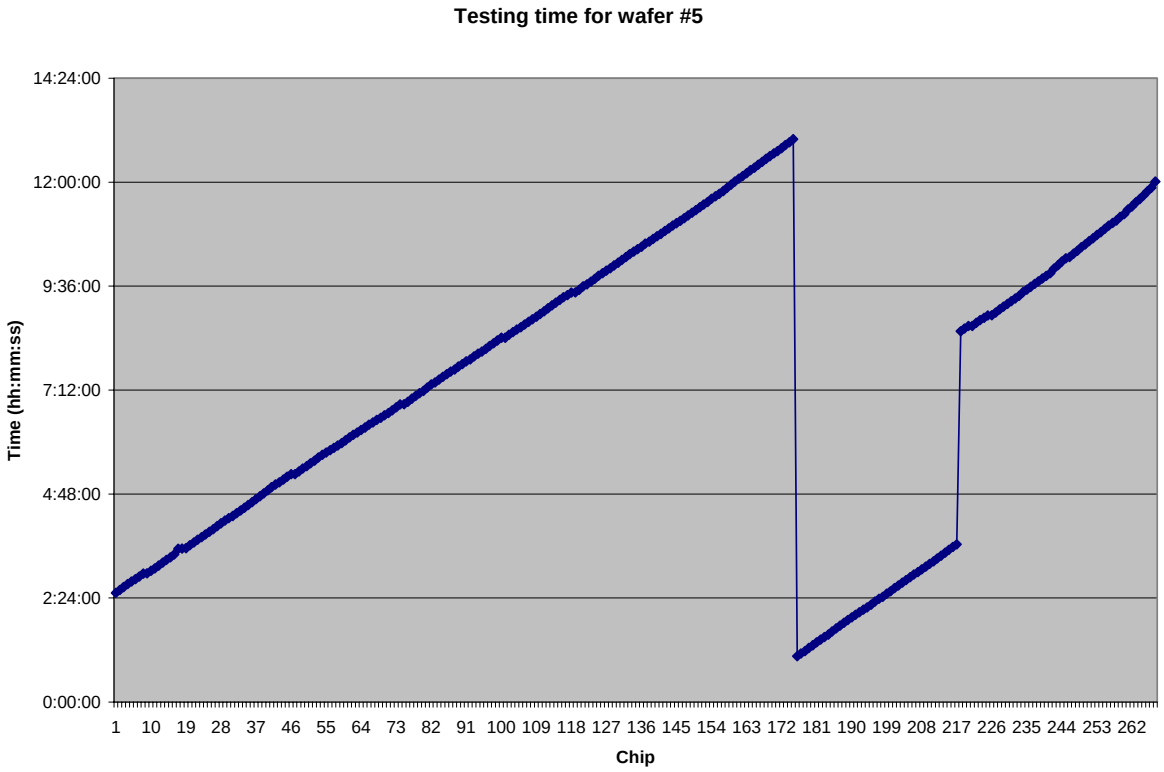

Figure 13c Testing time on wafer#5

2.3 Charge readout level

A similar set of plots is shown in Figure 11a, b, c for the readout charge, which has also reported previously to have a somehow large variation, although there is no specification. Note that our ADC used to digitize the analog output of the PSI chip has a sensitivity of ~0.5mV differential input voltage per ADC count (2V full range for a 12 bit ADC). The data plot in Figure 11 shows a charge variation within a chip (from pixel to pixel) of ~200 counts or ~ 100mV. On a full wafer the readout charge may vary up to ~600 counts or ~300mV. Similarly, from Figure 10, each of the six address levels variation within a chip is ~100 counts or 50mV and on the full wafer is ~200 counts or ~100mV.

It is worth to note that currently there is no special test that checks the PSI chip from the charge readout point of view. Also PSI group is not doing any charge and analog level measurements, as far as we are aware of. Their test program runs the PSI46V2 chip at a clock frequency of 10 MHz, instead of 40 MHz as we are doing.

The above statistics include only the 'perfect' chips. If we sort the tested chips based on the number of failed pixels, we obtain the graphics shown in Figure 12a, b and c. The total number of chips on each wafer is slightly larger than 4*62=248 because the wafer report file that I used contains also the chips that were retested (see following discussions). It can be concluded that ~160/248=65% of the chips are 'perfect' and ~200/248=80% of the chips have less than 100 pixels failed. The failure type will be discussed shortly. The bottom line is that these three wafers have by far much higher yield than previous PSI46V2 wafers.

2.4 Wafer testing time

Another set of plots presented in Figure 13a, b and c shows the test time. For example wafer#4 test time in Figure 13b starts at ~4:00PM and ends the next day at ~7:00AM. The following dots in the graph are chips measured a second time in manual mode.

2.5 PSI vs. FNAL test results comparison on chips with strong disagreement

Two of the three wafers we tested (#4 and #5) were previously tested at PSI. Each of the 248 chips on these two wafers was manually checked for agreement between the two testing groups. The chips were distributed in three categories:

1. Perfect agreement. These chips require not further discussion.
2. Strong disagreement. These chips are discussed in this section.
3. Slight disagreement. These chips are discussed in the next section.

Note that this classification as well as the following discussion is subject to human interpretation and my level of understanding of chip functionality importance.

Table 1.1 lists the chips found in strong disagreement on wafer #4. Table 1.2 is the same for wafer #5. Some of the chips were tested a second time, see "Fermi test#2" column. The column "P/F/M" lists my qualification for chip usage as Pass, Fail or Marginal. The column "Y/N" qualifies the agreement between PSI and FNAL tests as I see it. All tests (see Section 1) are performed at 40MHZ, except the time stamp buffer test which is done at 10MHz (see Section 1.5). There is also a last column with results when the chip is run at 20MHz instead of 40MHz. The reason for this frequency change will be explained shortly.

Some mnemonics are used to shorten the failure type description, as follows:

1. DBT stands for Data Buffer Test errors.
2. TSBT stands for Time Stamp Buffer Test errors.
3. N1, N2 and N3 stand for pixels not responding at first, second or third trim bit settings inside the pixel loop test as described in Section 1.7. The masktrim settings used are 0x84, 0x88 and 0x8C respectively, while the vcalmin=0x40, vcalmax=0xC0 and vcalstep=0x10.
4. F, FD stands for FIFO overflow when pixel is enabled respectively disabled. Usually a FIFO overflow is accompanied by a chip oscillation. The reverse statement is always true.
5. D stands for pixel responding when disabled.
6. L stands for pixel responding with wrong address levels.

Chip	PSI test	Fermi test#1	Fermi test#2	P/F/M	Y/N	Fermi test#3 @ 20MHz
1-0	2-4 dcol	Oscillation from col 10 to 52	same	F	N	same
1-2	1 dcol	3897 N1N2N3	same	F	N	26N,L
2-2	>30 pixels	Idig=60mA, 1428N3	Idig, Oscill.	F	N	1914L
2-3	1 pixel	OK	OK	P	Y-	OK
5-3	>30 pixels	1pixel(C47,R25)		P	Y-	same pix
14-2	OK	OK but all DBT failed		M	N	OK
16-1	1 pixel	4160N1N2N3	4160N1N2N3	F	N	37N3
24-2	>30 pixels	1pixel(C45,R30)	same pixel	P	Y-	same pix
28-0	OK	OK but some DBT and TSBT	same	M	Y-	OK
28-1	1 dcol	Oscillation and multiple hits	same	F	N	same
31-0	OK	4160N1N2N3	same	F	N	OK
31-1	1 dcol	Oscillation from col 25 to 52	same	F	N	same
37-1	2-4 dcol	Idig=40mA, 4160N1N2N3		F	N	same
38-3	OK	OK but many DBT errors	same	M	Y-	OK
41-2	>30 pixels	22N3 + all TSBT failed		F	N	5N3N2N
42-1	>30 pixels	OK	OK	P	Y-	OK
43-1	1 pixel	OK	OK	P	Y-	OK
50-0	OK	4160N1N2N3	same	F	N	OK
50-1	1 pixel	1458N3 + DBT + all TSBT		F	N	OK

50-2	OK	OK but one TSBT(dcol 24)	same	P	Y-	OK
52-2	Short	Idig=53mA 1110N,D	see pix map	F	Y	same
53-0	2-4 dcol	Idig=75mA 4160N1N2N3	same	F	N	same
54-0	2-4 dcol	Idig=75mA 4139N,F,FD	same	F	N	same
54-1	2-4 dcol	Idig=50mA 3492N,F,FD,D,L	see pix map	F	N	same
56-3	1 dcol	806N1N2N3 + few DBT	see pix map	F	N	same
57-0	OK	19N3 + all TSBT		F	N	OK
62-3	OK	4160N1N2N3		F	N	1N3

Table 1.1 Wafer #4 (XN4F4YT) test result comparison between PSI and FNAL. Only chips in category 'strong disagreement' are listed.

Chip	**PSI test**	**Fermi test#1**	**Fermi test#2**	**P/ F/ M**	**Y/ N**	**Fermi test#3 @ 20MHz**
1-1	3-9 pixels	OK	OK	P	Y-	OK
5-1	1 dcol	4160F,FD	same	F	N	Oscillate
10-1	1 pixel	OK	OK	P	Y-	OK
13-2	>30 pixels	2N1N2N3(18,80+49,44)	same 2 pix	P	Y-	same pix
14_1	>30 pixels	3N1N2N3	same 3 pix	P	Y-	same pix
14-2	>30 pixels	1 dcol N1N2N3 (col9+10)		M	N	same dcol
20-1	OK	3348N3+manyDBT and TSBT	same	F	N	OK
21-1	OK	4160N3N2N1	same	F	N	OK
23-2	OK	4160N3N2N1	same	F	N	1N3
26-3	I<5mA	Idig=25mA, Iana=24mA, OK	same	P	N	same, OK
31-0	OK	4160N1N2N3	same	F	N	13N3
35-0	OK	4160N3N2N1	same	F	N	OK
49-2	OK	4142N3N2N1		F	N	OK
50-2	>5 dcol	Idig=65mA,Iana=48mA,4160d	same	F	N	same
56-3	OK	Idig=41mA + 319N3		F	N	OK
60-1	OK	259N3 + many TSBT	same	F	N	212N3

Table 1.2 Wafer #5 (XM4F4ZT) test result comparison between PSI and FNAL. Only chips in category 'strong disagreement' are listed.

Note that the PSI test report is not saying explicitly the type of pixel defect. Also we can not infer from their defect list when some other defects, not pixel related (like TSBT, DBT), occurred.

MAIN COMMENTS.

1. We found chips that are oscillating, thus can not be measured with the current settings of DAC registers.
2. We found chips with high digital current (Idig>50mA) and with almost all pixels not responding but qualified with just 2-4 dcol defects by PSI. We found also one perfect chip (26-3 on wafer #5) that is qualified as I<5mA by PSI.

3. We found chips that either have all 4160 pixels not responding at all (N1N2N3) or have some responding pixels but experience other defects like DBT of TSBT, but were reported by PSI as perfect chips.
4. Finally we found also four chips (42-1 and 43-1 on wafer#4 and 1-1 and 10-1 on wafer#5) that are perfect in our test but are reported with different number of defect pixels by PSI.
5. As a summary, the 27 chips listed in Table 1.1 represent ~11% of wafer#4. The 16 chips listed in Table 1.2 represent ~6% of wafer #5. But when we do the test at 20MHz from the 27 chips with strong disagreements listed in Table1.1 we go down to only 15 chips or ~6% of wafer#4. Similarly for wafer#5 we go down from 16 to 8 chips with disagreements.

There is more that can be commented on each chip listed above. The reader is invited to do its own analysis and interpretation. Sometimes the pixel map distribution might suggests some interpretation, as is chip 52_2 on wafer#4 with a partial pixel map shown in Figure 14a or Figure 7b representing the pixel map of chip 44_1 from wafer#5. Please go back and look careful at the pixel map defect distribution on Figure 7b since all N3 type failures we will investigate in next Section 2.6 show this layout distribution. Just for reference see also Figure 14b and 14c with some other 'nice' patterns.

Anyway, an overall conclusion might be that, although the number of chips with disagreement is reasonable low (6 to 11%) there are some defect type (see comment 2 above, power supply current) **for which we SHOULD NEVER see any kind of disagreements**.

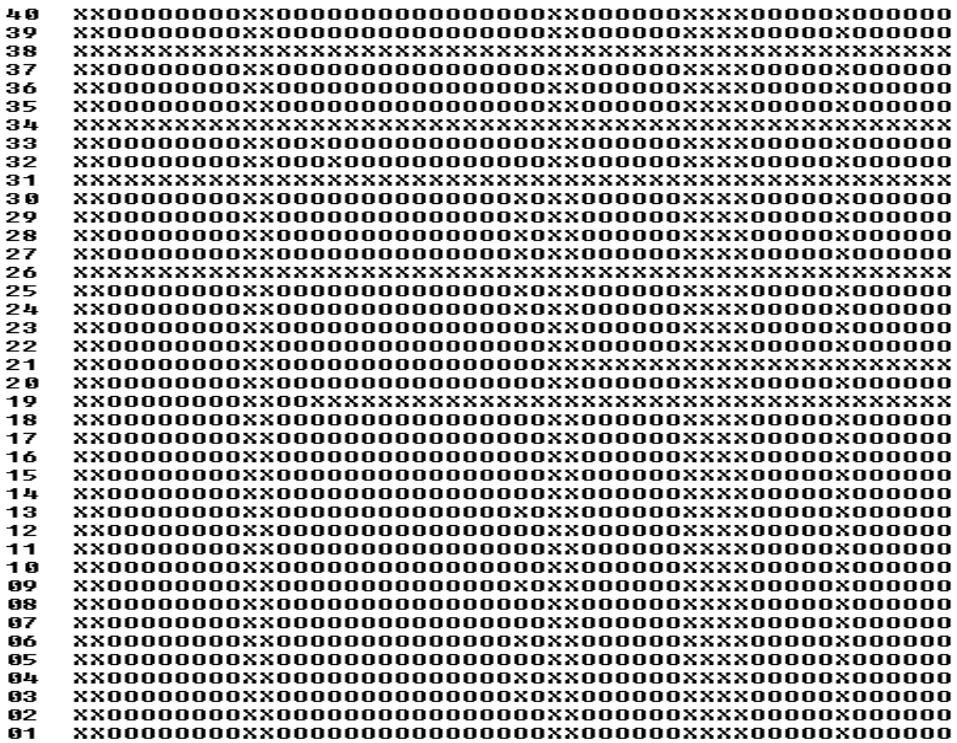

Figure 14a Partial pixel map of chip 52_2 on wafer#4

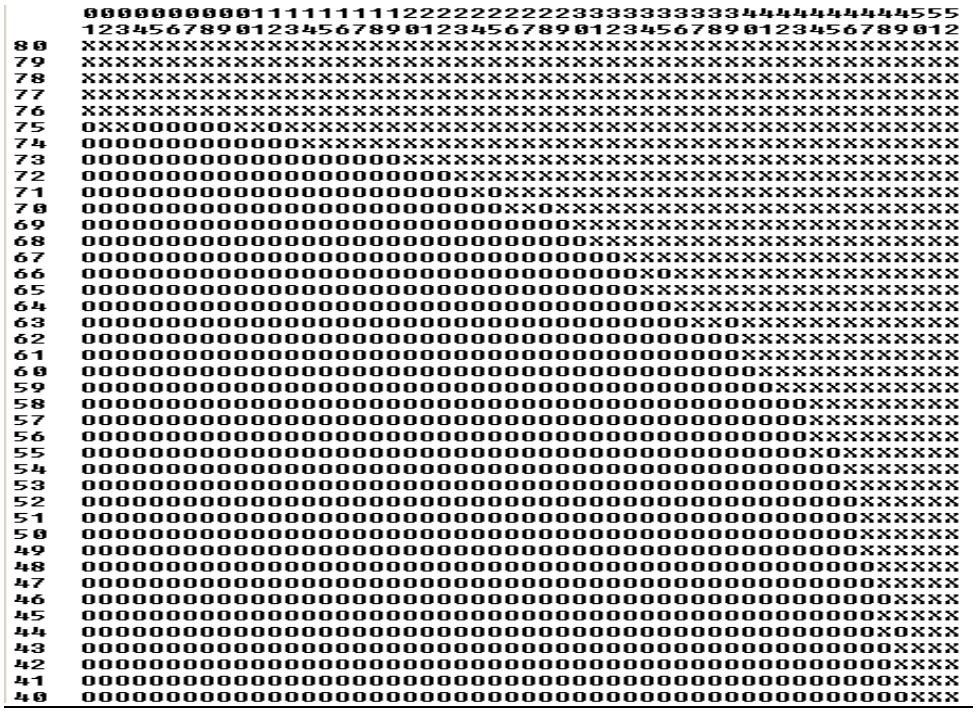

Figure 14b Partial pixel map of chip 56_3 on wafer#4

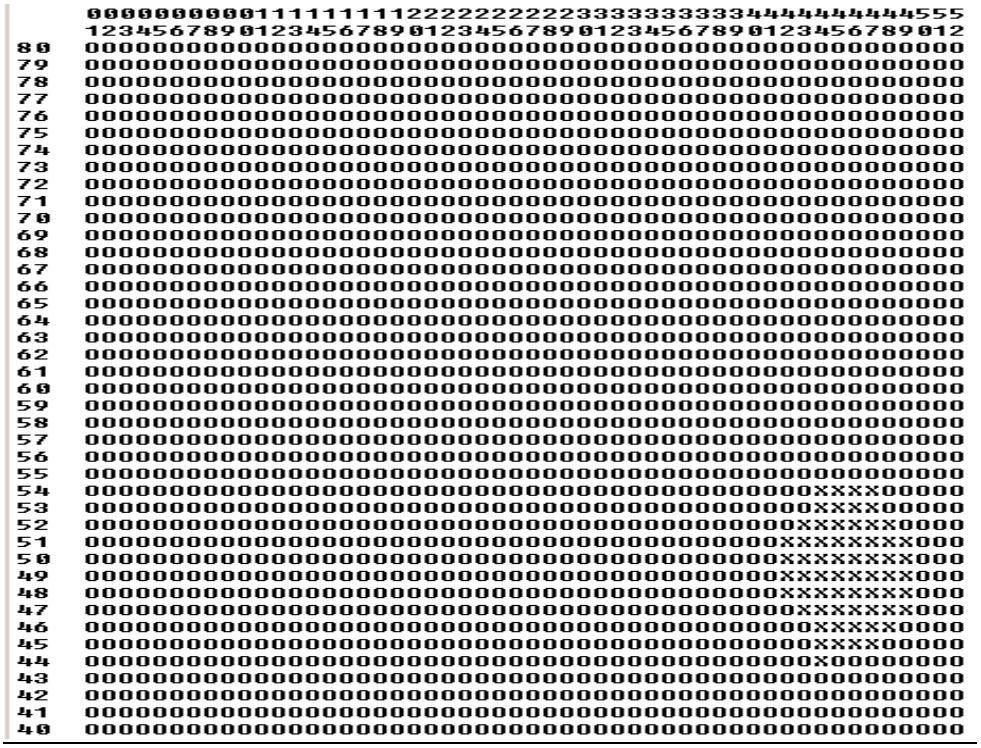

Figure 14c Partial pixel map of chip 43_3 on wafer#5

2.6 PSI vs. FNAL test results comparison on chips with slight disagreement

Following the classification from Section 2.5, this section will focus on chips with so called 'slight disagreement'. This includes all chips that are neither in perfect agreement nor in strong disagreement. It turned out that all these chips have just one type of defect. This is an 'N3' type defect which means that, while each pixel is measured following the masktrim and Vcal double loop explained in Section 1.7, the pixel is not responding at the third masktrim value (in our text that value is 0x8C) regardless of the Vcal value (in our test that is swept between 0x40 and 0xC0 in step of 0x10). The chips falling in this category are shown in Table 2.1 and 2.2 for wafer#4 and wafer#5 respectively.

Chip	PSI test	Fermi test#1	Fermi test#2	P/F/M	Y/N	Fermi test#3 @ 20MHz
2-0	OK	Few TSBT	same	P	Y-	2N3
9-0	OK	1N3		P	Y	OK
9-1	10-29pixels	4N3	5N3	P	Y	1N1N2N
10-1	OK	7N3		P	Y	OK
11-1	OK	4N3		P	Y	OK
12-2	OK	82N3		P	Y	OK
13-1	OK	1N3		P	Y	OK
15-1	OK	145N3 + few TSBT		P	Y	15N3
15-2	OK	1224N3 + few DBT		M	Y-	OK
17-0	OK	1021N3 + few DBT		M	Y-	OK
17-3	1 pixel	1373N3 + few DBT		M	Y-	1pix(9,13)+ 3N3
18-2	OK	664N3	848N3	M	Y-	OK
18-3	OK	1N3		P	Y	OK
20-1	OK	8N3		P	Y	OK
21-1	OK	1129N3 + some DBT,TSBT	same	M	Y-	234N3
21-2	OK	2240N3 + some DBT		M	Y-	OK
21-3	OK	755N3		M	Y-	OK
23-0	OK	131N3 + few DBT		P	Y	9N3
23-1	1 dcol	1dcol (25,26) + 17N3		M	Y	same dcol
23-3	OK	74N3		P	Y	OK
25-3	1 pixel	1853N3 + some DBT		P	Y	1pix(49,73)
26-2	OK	1N3		P	Y	OK
32-0	OK	53N3		P	Y	OK
32-1	OK	250N3		P	Y	3N3
34-0	OK	2141N3 + some DBT		M	Y-	OK
35-0	OK	4142N3		M	Y-	OK

36-2	OK	14N3		P	Y	OK
37-2	OK	635N3		M	Y-	OK
37-3	OK	5N3		P	Y	OK
40-0	2 pixels	8N1N2N3+513N3+few DBT		M	Y-	OK
41-1	OK	785N3		M	Y-	1L(18,60)
41-3	OK	76N3		P	Y	OK
42-0	OK	574N3 + DBT + TSBY	same	M	Y-	798N3+ DBT
43-2	OK	1N3		P	Y	OK
44-3	OK	61N3		P	Y	OK
45-0	OK	1262N3 + some DBT	same	M	Y-	OK
45-2	OK	600N3		M	Y	OK
46-0	OK	1N3		P	Y	OK
46-1	OK	3910N3		M	Y-	OK
46-3	OK	1646N3 + few DBT	same	M	Y-	OK
48-1	OK	1N3		P	Y	OK
49-1	OK	211N3		P	Y	OK
49-2	1 pixel	81N3N2N1(col35+36)+DBT	same	M	Y-	Oscillation
50-3	OK	162N3 + all TSBT		M	Y-	44N3
51-3	2-4 dcol	1361N,L,D+DBT+TSBT	see pix map	M	Y-	same
53-1	1 dcol	1 dcol(col37,38)+other48 pix	see pix map	M	Y	same
54-3	OK	1438N3 + few DBT		M	Y-	157N3
55-0	1 pixel	1903N3 + some DBT		M	Y-	OK
58-0	OK	2617N3 + some DBT		M	Y-	OK
58-2	OK	4122N3 + many TSBT		M	Y-	OK
60-0	OK	20N3		P	Y	10N3
60-3	OK	6N3		P	Y	OK
61-1	1 pixel	298N3		P	Y	OK

Table 2.1 Wafer #4 (XN4F4YT) test result comparison between PSI and FNAL. Only chips in category ‘slight disagreement’ are listed.

Chip	**PSI test**	**Fermi test#1**	**Fermi test#2**	**P/ F/ M**	**Y/ N**	**Fermi test#3 @ 20MHz**
1-0	OK	1N3		P	Y	OK
1-2	OK	191N3 and L(col9,10)	same	P	Y	1788L
2-1	OK	3998N3		M	Y-	OK
2-2	OK	2590N3 + some DBT	same	M	Y-	OK
3-3	OK	82N3		P	Y	OK
4-2	OK	1080N3		M	Y-	OK
5-2	OK	2572N3 + some DBT	same	M	Y-	OK

7-1	OK	2N3		P	Y	1pix(52,80)
9-2	OK	2022N3 + some DBT		M	Y-	OK
10_0	1 dcol	1dco(29,30)+2042N3+DBT		M	Y-	same dcol
10-2	OK	1006N3 + few DBT		M	Y-	3N3
10-3	OK	1089N3 + few DBT		M	Y-	6N3
11-3	OK	732N3 + few DBT		M	Y-	OK
13-3	OK	326N3 + DBT + TSBT	same	M	Y	same
15-3	1 pixel	1 pixel (50,59) + 2N3		P	Y	same pixel
18-3	OK	8N3		P	Y	10N3
19_0	OK	1N3		P	Y	1N3
19-3	OK	58N3		P	Y	OK
21-0	OK	102N3		P	Y	OK
21-2	OK	140N3		P	Y	OK
22-0	OK	3003N3 + few DBT		M	Y-	OK
22-3	OK	2N3		P	Y	same pix
23-3	OK	1N3		P	Y	OK
26-0	OK	3N3		P	Y	OK
28-2	OK	3561N3 + many DBT		M	Y-	3N3
28-3	OK	2N3		P	Y	OK
29-0	OK	3547N3 + many DBT		M	Y-	OK
30-3	1 pixel	1pixel(42,1)+2pixM	3M	P	Y	1N,2M,2L
31-2	OK	6N3		P	Y	OK
31-3	1 pixel	4N1N2N3 in col 26 + 170N3		P	Y-	OK
32-3	>30 pixels	52 defects, all in R57	see pix map	P-	Y	same
33-2	OK	1N3		P	Y	OK
33-3	OK	15N3		P	Y	OK
34-3	OK	158N3		P	Y	OK
36-0	OK	1763N3 + few DBT		M	Y-	OK
38-2	OK	42N3		P	Y	OK
39-0	OK	1883N3 + some DBT		M	Y-	OK
39-3	OK	3181N3		M	Y-	OK
40-0	OK	4092N3		M	Y-	OK
40-2	OK	2038N3 + some DBT		M	Y-	OK
41-0	OK	26N3		P	Y	1N3
41-3	OK	2634N3 + some DBT		M	Y-	OK
24-3	OK	1N3		P	Y	OK
43-0	OK	1N3		P	Y	OK
43-3	>30 pixels	93N1N2N3 + 25N3N2N1	see pix map	P-	Y	67N3
44-1	OK	793N3 (see Figure 7b)		M	Y-	OK
44-2	OK	3N3		P	Y	OK
45-3	OK	1071N3		M	Y-	OK
47-2	OK	1N3		P	Y	OK
47-3	OK	2N3		P	Y	OK
49-3	OK	3186N3 + DBT		M	Y-	OK

50-0	OK	1510N3 + some DBT		M	Y-	OK
50-1	OK	3897N3		M	Y-	OK
53-3	OK	1L	2L + 36N3	P-	Y	OK
55-0	OK	15N3		P	Y	OK
55-3	OK	977N3		M	Y-	5N3
56-1	>30 pixels	127 in col7+8 with L or N	same	P-	Y	Oscillation
58-2	OK	4086N3		M	Y-	OK
58-3	1 pixel	1 pixel (25,1) + 128N3		P	Y	1pix(25,1)
62-3	OK	24N3		P	Y	OK

Table 2.2 Wafer #5 (XM4F4ZT) test result comparison between PSI and FNAL. Only chips in category 'slight disagreement' are listed.

MAIN COMMENTS.

1. There are 53 chips listed in Table 2.1 or ~21% of wafer#4 and 60 chips listed in Table 2.2 or ~24% of wafer#5. But after the test is repeated at 20MHz, the number of chips with slight disagreement went down to 15 or ~6%) of wafer#4 and 13 or ~5% of wafer#5 respectively.
2. The number of pixels with N3 failure can be anywhere between 1 and 4160. This number is not repeating exactly if the chip is retested, but the failed pixels reside almost around the same locations (columns and rows) in the pixel map. Hint: all chips have a pixel map distribution like the parabolic type shown in Figure 7b. The failed pixels are located in the upper side of a column, with more pixel failures on columns situated toward the left and right side of the chip and less pixel failures on columns situated toward the center of the chip, thus following a parabolic type distribution. **We suspect that this is due to calibration voltage circuit and its network distribution layout.** It is hard to say that either the circuit design or the processing variations are responsible for this. We do believe that in fact both of them have some contribution. Anyway, the chip designer is invited to investigate and comment this behavior.

There are a couple of things that I tried in order to investigate this N3 type of failure and these are presented in the following subsections. All the measurements that follows were done on chip 3-3 from wafer#5 (see Table 2.2) which has ~80N3 defect pixels.

2.6.1 Adjusting the Vthcomp DAC register setting.

It make sense to believe that by lowering the threshold value the pixels will become more sensitive so they will 'fire' also at the highest masktrim value (remember N3 is the last masktrim value in the pixel test and it corresponds to 0x8C setting). Note that increasing the Vthcomp settings means in fact lowering the threshold. Unfortunately this approach didn't work as can be seen from data in Table 3. When the threshold was lower (settings>0x40) the pixels become sensitive to noise and apparently do not respond at all (N1N2N3). This can be due to a large number of pixels firing on noise and overflowing (reset) the data buffer or time

stamp buffer. On the other hand, when the threshold is higher (settings<0x40), more pixels fail at N3. It seems to be no available setting that will cancel the N3 failure type

Nr.crt.	Vthcomp (hex)	Test results
1	0x30	4160N3
2	0x38	3241N3
3	0x40 (default)	97N3
4	0x42	195N1N2N3
5	0x44	101N1N2N3
6	0x48	95N1N2N3
7	0x50	127N1N2N3
8	0x60	162N1N2N3

Table 3 Adjusting Vthcomp DAC register settings

2.6.2 Adjusting the Vtrim DAC register setting.

Similar test results while adjusting Vtrim register are shown in Table 4. Also in this case it is difficult to draw a conclusion. Small values of Vtrim are known to 'wrap' together the sensitivity curves for different trim bits. Large values of Vtrim are known to 'spread apart' the sensitivity curves for different trim bits. The last one translates according to data in Table 4 in a larger number of pixels not responding at all N1N2N3. Anyway, the N3 failure is still there for all Vtrim settings exercised.

Nr.crt.	Vtrim (hex)	Test results
1	0x20	279N3
2	0x30	250N3
3	0x40 (default)	238N3
4	0x50	125N1N2N3
5	0x60	206N1N2N3

Table 4 Adjusting Vtrim DAC register settings

2.6.3 Investigating the trim bits values

It makes sense to think that maybe this N3 failure is due to defect trim bits in the pixel unit cell. Table5 shows the test results for four different masktrim ranges. In these four tests the trim bits are varied from 0 to 3 (first test) then from 4 to 7 (second test) then from 8 to 11 (third test) and finally from 12 to 15 (fourth and last test), in increment of one count. The failure type results are mixed and it is difficult to draw a conclusion.

Nr.crt.	masktrim (hex)	Test results

1	0x80,81,82,83	25N4N3N2N1
2	0x84,85,86,87	178N4N3N2N1
3	0x88,89,8A,8B	54N4,N3N2N1
4	0x8C,8D,8E,8F	1123N4

Table 5.1 Adjusting the pixel unit cell masktrim settings

A common observation is that in all these tests the N3 failed pixels were always in the upper left corner of the pixel map. Even more, when failure type N1N2N3N4 occurs, all pixels are clearly grouped in the right column of each double column. It seems that the last ~20 rows of the columns are more likely to fail. This brings again the idea of a fail mechanism correlated somehow with pixel position. This is not a particular chip situation since, as pointed above in comment #2, all chips that present N3 failure have this parabolic shape of the pixel map distribution, for both wafers. The natural candidate to suspect for this is the calibration and/or injection network which might not distribute evenly the voltage across all pixel unit cells. This can be a design limitation or can be a wafer processing problem like polisilicon interconnection resistivity to high.

Another disappointing result was the following. Probing a previously tested good chip, say 4_0 (on the same wafer#5) and repeating the trim bits test we found that the so called good chip is now failing in some cases, as shown in Table 5.2

Nr.crt.	masktrim (hex)	Test results
1	0x80,81,82,83	OK
2	0x84,85,86,87	62N1N2N3N4 in col 2,4,6
3	0x88,89,8A,8B	OK
4	0x8C,8D,8E,8F	82N1N2N3N4 in col 2,4,6,10,12

Table 5.2 Adjusting the pixel unit cell masktrim settings for a ‘good’ chip 4_0.

2.6.4 Pixel threshold curve

We leave for a moment the testing program and do the following two measurements presented here and in Section 2.6.5. These two tests are measurements of the Vcal at which pixel fires and of the readout charge, both as a function of pixel position within a double column.

Set the pixel to be measured to one with pc=pixel column and pr=pixel row, where pc=0 or 1 and pr=0, 20, 40, 60, 79 (both number are decimal). We want to investigate the pixel threshold dependence on his position inside a column. The measurement data is presented in Figure 15. The masktrim bits are varied from 0x82 to 0x8E in step of 0x02. At each masktrim value, the Vcal is varied between 0 and 236 (decimal) in step of 4 counts. At each Vcal, the pixel is triggered 16 times for a better statistic of the threshold. The process is repeated for all seven masktrim values and for all five pixel rows values inside a column.

The data is plotted as a family of curves in Figure 15. Each pixel cell from column pc and row pr shows a nice linear dependence of Vcal threshold w.r.t. trim bits settings. But Figure 15 also shows a large variation from pixel to pixel. The variation range along the 10 measured pixels inside the first double column is plot in Figure 15 as a thick black line. It can be seen that the Vcal at which the pixel 'fires' varies inside a double column from 46 counts when masktrim=0x82 to 72 counts when masktrim=0x8E. All the time, the higher the pixel row number, the larger the Vcal required to fire the pixel. The difference between the 10 measured pixels is as high as 118 Vcal counts over all masktrim bits or as high as 72 Vcal counts for a constant masktrim setting. These are quite large numbers considering the full Vcal range of 255 counts.

Based on these measurements we can say that the parabolic shape of the pixel map failures is certainly due to the higher Vcal values required by pixels placed up in the column. This again suggests the lack of capability on calibration voltage and/or network distribution layout.

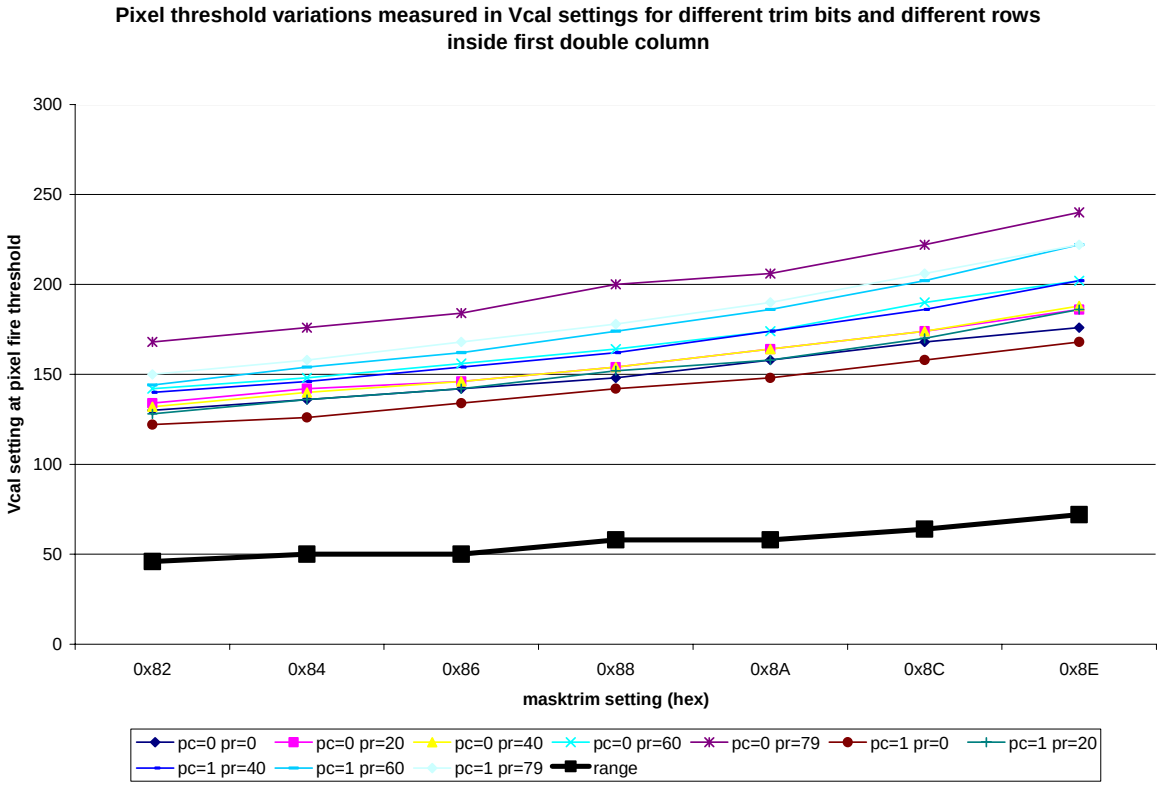

Figure 15 Pixel threshold variation inside first double column for chip 3-3

Figure 15 reveals also that a vcalmax=0xC0=dec192 which was used in our automatic test is not enough to fire the pixel if masktrim>0x8A. This last observation partially explains the N3 failure we are investigating here. And I say partially because I went back to the full testing program and changed the Vcal range to be higher, between 136 and 248. Detailed print of all pixels data (not shown here) correlates very well with Figure 15, but only when

pixel row is less than ~60. For higher row numbers, the Vcal in Figure 15 is about 20 counts lower than the one required during the automatic test program, or the test program fails in finding the pixel firing.

2.6.5 Pixel charge variation

A last measurement that further confirms the idea that the N3 failure mechanism is related to problems in calibration voltage and/or network distribution layout non uniformities is the following one. For the same five pixels used in previous section (located at pc=0 and pr=0, 20, 40, 60 and 79) the charge readout was measured when masktrim=0x82 and the Vcal was incremented in step of 4 counts between decimal 0 and 236. For each Vcal settings the pixel response was measured over 100 triggers for a good statistic measurement. The min, max and average values were calculated. The range found (max-min) was about 20 counts. Figure 16 is a plot of the average measured charge for only five of the Vcal settings.

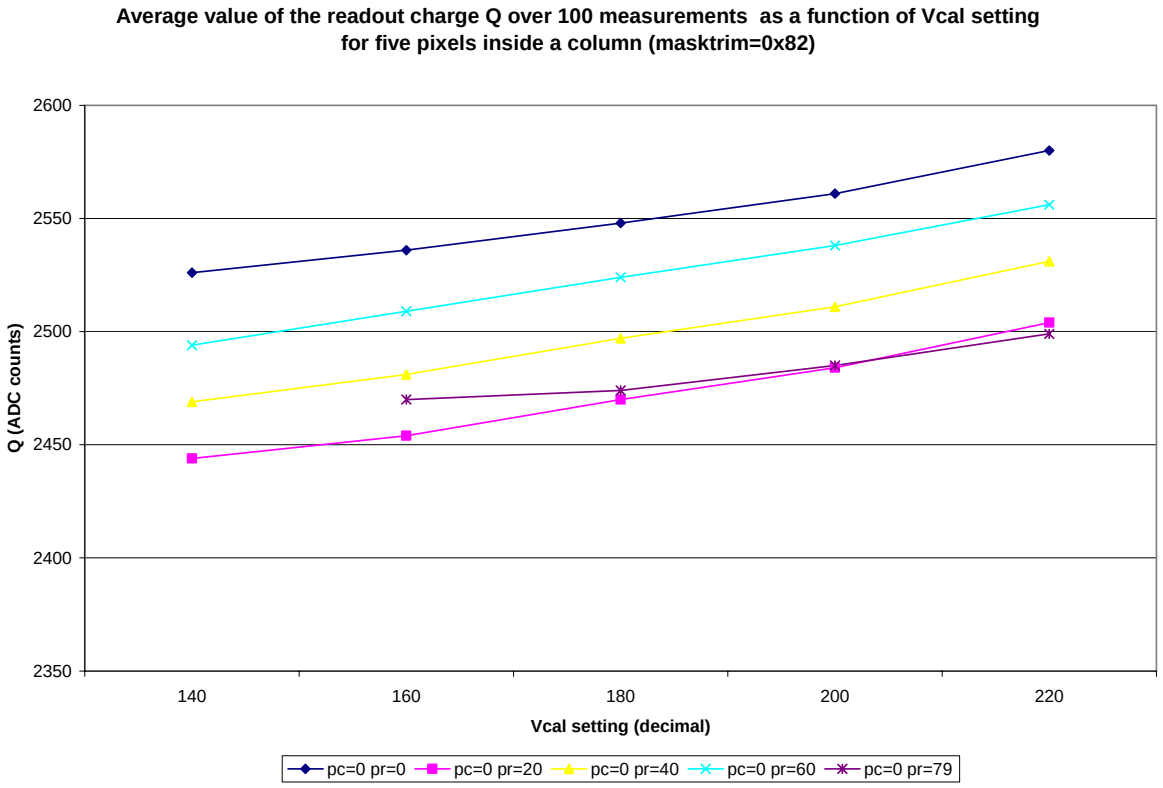

Figure 16 Pixel charge variation inside first double column for chip 3-3

The dependence of the (average) readout charge on Vcal setting is almost linear. For further linearity study and/or charge dependence on miscellaneous chip settings see my previous test report from February 2005. What is important for our N3 failure type study is the variation range of the four lines in Figure 16 which is about 80 ADC counts in charge

variation for the 5 pixels investigated, regardless of the actual charge injected (i.e. actual Vcal setting). Over all 80 pixels in a column this variation might be larger. One of the main contributions to this variation, in my opinion, can be related to, for example, non uniformity in charge calibration voltage (due to different pixel loading effect on the voltage generator or due to interconnection resistivity variations) or nonuniformities in the charge injection capacitor from pixel to pixel or other matching tolerances of specific circuitry inside the pixel unit cell.

All the above tests support the assumption that the N3 failure mechanism is related with problems in calibration voltage and/or network distribution layout non uniformities.

2.6.6 Changing the test frequency from 40MHz to 20MHz

One of the last experiments we did was just running the full test program at 20MHs instead of 40MHz. This was done for all wafers, but only on chips with disagreement. The results are presented in the last column of Tables 1.1, 1.2, 2.1 and 2.2. The improvement is significant when we compare with PSI test results at 10MHz. Some N3 type failures are still there suggesting that if we'll do the chip test at 10MHz we'll have very likely a perfect agreement.

2.7 FNAL test results for wafer#3

For this wafer there are no PSI test results to do a data comparison. The results of our testing are summarized in Table 6, for all chips which have at least one type of defect. In the same manner as we did for wafer#5 and wafer#4, Table 6 lists the chips with at least one type of failure. The columns labeled test#1, test#2 and test#3 have the same meaning as for the other two wafers (i.e. the test was done in the same conditions). But there is a new column labeled test#4.

This test#4 is performed at 40MHz clock frequency but with a new value of VcalDel register setting. All the other tests and wafers were using VcalDel=0x58. For this wafer#3 and this test#4 we did first few manual measurements to find out what is the VcalDel range for which one random pixel fires. This is similar with the measurement described in slide 35 from November 2004 report. We found the range to be roughly from 0x28 to 0x60. This shows that our value of 0x58 was somehow on the edge of the interval and that may be also a source of not responding pixels, regardless of the calibration voltage circuit and its network distribution layout issues discussed in previous section. It is also possible that some other register settings are also on an edge. So we set VcalDel=0x40 (0x44 is the average of 0x28 and 0x60) and repeat the test at 40MHz.

Chip	Fermi test#1	Fermi test#2	P/ F/ M	Fermi test#3 @ 20MHz	Fermi test#4 @40MHz VcalDel=0x40
2-2	3203N3 + DBT + TSBT		M	OK	OK
2-3	3688N3 + DBT + TSBT		M	OK	OK
3-3	4160N1N2N3	same	F	same	same
4-0	Oscillation from col 10 to 52	same	F	1N1((9,37)	same 1N1 + all DBT failed
4-1	78L in col 27+28	same	M	4000L	78L in col 27+28
4-3	23N3		P-	OK	OK
5-0	Idig=200mA		F	same	-----
5-2	Idig=68mA, 71N3 + DBT		F	same	same
6-0	4160N1N2N3	same	F	1pix(23,38)	1pix(23,38)
8-1	Oscillation from col 44 to 52	same	F	same	-----
8-3	Idig=90mA		F	same	-----
11-0	1049N3 + DBT		M	OK	OK
11-2	137N3 + DBT + TSBT		M	OK	OK
12-1	Idig=7mA, Iana=0mA		F	same	-----
13-1	111N3+L in col 33+34	same	M	106L(col33,34)	105L(col33,34)
17-0	122L in col 1+2	OK	P-	OK	OK
17-1	3779 N3 + DBT + TSBT	same	M	OK	OK
17-3	67N3+L	same	M	OK	OK
18-1	Idig=250mA, Iana=1mA		F	same	-----
19-0	17N3		P-	2pix(1,57)(7,36)	2pix(1,57)(7,36)
20-3	600N3		P-	OK	OK
22-1	Idig=100mA		F	same	-----
22-3	4160N3N2N1 + DBT + TSBT		F	same	same
23-1	160 N1N2N3 in col 15+16		P-	same dcol	same dcol
25-2	Idig=94mA		F	same	-----
26-2	1019L in col 1 to 13	4160L	F	OK	OK
27-0	1214L in col 1 to 16	2888L	F	OK	OK + all DBT failed
27-2	4039N3		M	OK	OK
28-1	113N1N2N3 in col 31+32		P-	113 in same col	Osc. from col 31
28-3	65N1N2N3 col 39+40 Id=50m		P-	47N123 in col 40	3L in col 39 + 47N in col 47 + all(DBT+WBC)
29-0	1N1N2N3(38,26) + all DBT	same	F	1pix(38,26)	1pix(38,26) + all(DBT+WBC)
29-1	Idig=250mA, Iana=1mA		F	same	-----
29-2	Idig=9mA, Iana=0mA		F	same	-----
29-3	3613N3 + DBT + TSBT		M	OK	1N3
30-1	2N1N2N3 in col 37 row 1,2	same	P-	2pix(37,1)(37,2)	2pix(37,1)(37,2)

30-3	**1069N3 + DBT**		**M**	**OK**	**1N3**
31-0	**1725N3 + DBT**		**M**	**5N3**	**8N3+fewTSBT**
31-1	**Idig=84mA**		**F**	**same**	**-----**
31-2	**61N3**		**P-**	**23N3**	**26N3+fewTSBT**
32-0	**4160L,N**	**542N3**	**M**	**OK**	**OK**
32-1	**Idig=77mA, 3010N3N2N1**		**F**	**same**	**-----**
32-2	**Idig=83mA, 2N3**		**F**	**Idig=96mA, OK**	**Idig=96mA, OK**

Table 6 Wafer #3 (XT4EF6T) test result. No comparison between PSI and FNAL is available for this wafer. All chips in category 'strong disagreement' or 'slight disagreement' are listed.

As we can see from Table 6 the two last tests (#3 and #4) show quite similar results. Based on this we can say that the better results obtained at 20MHz (test#3 compared with #1 and #2) are not directly due to lowering the clock frequency but to the fact that the 0x58 setting for VcalDel is no more on the edge of the functional range since we know that at lower frequencies the range of VcalDel in which pixel is responding is wider. We can say the same thing in a different way: with the new VcalDel=0x40 and the frequency at 40MHz the chips do not fail at N3 because the third masktrim=0x8C is still inside the range of VcalDel for which the pixel responds. It might be that the N3 type failure (or say N4 type failure) becomes again an issue if the masktrim is increased to 0x8F, for example.

In fact we can see from Table 6 that some chips still have few number of N3 type failures. We can see also that chips like 4-0, 27-0, 28-3 and 29-0 have new failure modes like DBT (data buffer test) on all double columns and WBC test failure on all eight WBC numbers exercised. But overall this wafer#3 seems to have fewer problems than the other two. What is somehow strange is that all chips listed in Table 6 are in the first 32 reticules (lower half of the wafer) and everything is perfect on the upper half of the wafer! This is a good reason to question the process uniformity along this 8 inch wafer.

Conclusions

Three more PSI46V2 wafer were tested and analyzed from the failure mode point of view. Our testing program was completed with new procedures inspired from PSI group.

Some limitation of calibration voltage circuitry were discovered and for this reason **the time stamp buffer test is the only test that can't be done at 40MHz clock frequency.**

Comparison with PSI test results was done on two wafers. The disagreement between the two test results, although can be interpreted as basically being ~10% **should be improved.** Also, **there are failure types** (for example current supply related) **for which we should never see any disagreement.**

A new failure type was discussed thoroughly, although **the PSI designer's point of view will be very helpful in detailed understanding.** Based on our measurements we saw

that the fail pixels have a parabolic distribution within the chip area which was attributed mainly to the **calibration voltage circuitry and its network distribution layout.** We learned that we can 'hide' this effect either by lowering the frequency or by optimizing the VcalDel setting.

Some other testing issues like having all pixels enabled or disabled during testing or pixel's analog level variation for column and row encoding or for the output charge or, ultimately, having a chip parameters' data sheet for pass / fail qualification need further discussion with PSI and were not the subject of this report.

Some other tests may be added in the near future, like one which will **qualify the chip from the charge readout point of view.**

The overall yield of all three wafers is much higher than the previous PSI46V2 wafers **and this is certainly a big step ahead to production phase.**